57239

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Date 12/28/01 Serial # 09/863,737 Priority Application Date _____

Your Name M. Lewis Examiner # _____

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In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

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What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

12-28-01 A11:12 IN

If Use Only		Type of Search		Vendors	
cher:	Blalock, Derrick	Structure (#)		STN	✓
cher Phone:	306-0935	Bibliographic	✓	Dialog	✓
cher Location:	STIC-EIC2800, CP4-9C18	Litigation		Questel/Orbit	
Searcher Picked Up:	1/3/02	Fulltext		Lexis-Nexis	
Completed:	1/3/02	Patent Family		WWW/Internet	
her Prep/Rev Time:	60	Other		Other	
e Time:	117				

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SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2001/Dec W3
         (c) 2001 Institution of Electrical Engineers
*File   2: 50th issue for 2001 updated; next issues begin 2002 in January.
  File   6:NTIS  1964-2001/Jan W2
         (c) 2001 NTIS, Intl Cpyrght All Rights Res
*File   6: See HELP CODES6 for a short list of the Subject Heading Codes
(SC=, SH=) used in NTIS.
  File   8:Ei Compendex(R)  1970-2001/Dec W5
         (c) 2001 Engineering Info. Inc.
  File  34:SciSearch(R) Cited Ref Sci  1990-2002/Jan W1
         (c) 2002 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2001/Dec
         (c) 2001 ProQuest Info&Learning
  File  77:Conference Papers Index  1973-2001/Nov
         (c) 2001 Cambridge Sci Abs
  File  94:JICST-EPlus  1985-2001/Nov W3
         (c)2001 Japan Science and Tech Corp(JST)
*File  94: There is no data missing. UDs have been adjusted to reflect
 the current months data. See Help News94 for details.
  File  99:Wilson Appl. Sci & Tech Abs  1983-2001/Nov
         (c) 2001 The HW Wilson Co.
  File 108:AEROSPACE DATABASE  1962-2001/DEC
         (c) 2001 AIAA
*File 108: For update information please see Help News108.
  File 144:Pascal  1973-2001/Dec W4
         (c) 2001 INIST/CNRS
  File 238:Abs. in New Tech & Eng.  1981-2001/Dec
         (c) 2001 Reed-Elsevier (UK) Ltd.
  File 305:Analytical Abstracts  1980-2002/Dec W5
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*File 305: Frequency of updates and Alerts changing to weekly.
See HELP NEWS 305.
  File 315:ChemEng & Biotec Abs  1970-2001/Oct
         (c) 2001 DECHEMA
  File  14:Mechanical Engineering Abs  1973-2001/Nov
         (c) 2001 Cambridge Sci Abs
  File  65:Inside Conferences  1993-2002/Dec W5
         (c) 2002 BLDSC all rts. reserv.
*File  65: For variance in UDs please see Help News65.
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Set     Items   Description
S1        219   CI=(SI SS(S) O SS(S) F SS) (S)NE=4
S2        654   ((DIFLUOROSILANONE) OR (SILICON (W) OXYFLUORIDE) OR (SILIC-
                ON (W) FLUORIDE (W) OXIDE) OR (HEXAFLUORODISILOXANE) OR (OCTA-
                FLUOROTRISILOXANE OR SIOF OR SI(W)OXYFLUORIDE))
S3       9980   (FLUORINE OR F)(2N)(CONCENTRAT? OR PERCENT? OR PPM OR CENT
                OR WT OR WEIGHT)
S4    2447375   WIRE OR WIRES OR WIRING OR LINE OR LINES OR LINING
S5       2729   (WIRE OR WIRES OR WIRING OR LINE OR LINES OR LINING)(3N)(G-
                AP)
S6     188534   (INSULAT? OR OXIDE OR DIELETRIC) (3N) (FILM? ?  OR LAYER? -
                OR COAT????)
S7        853   S1 OR S2
S8          1   S7 AND S5
S9         93   S7 AND S4
S10        15   S9 AND S3
S11        31   S9 AND S6
S12        37   S8 OR S10 OR S11
S13        27   RD (unique items)
S14        27   S13 NOT PD>=20010523
S15         6   AU="ODA, NORIAKI"
S16        13   AU="ODA NORIAKI"
S17       621   AU="ODA N"
S18       443   E4-E7
S19        27   AU="IMAI, KIYOTAKA"
S20        37   AU="IMAI KIYOTAKA"
S21      1146   S15: S20
S22      1146   S21 NOT S14
S23         3   S22 AND S7
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T S23/3,AB/1-3

>>>No matching display code(s) found in file(s): 65

23/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6596855 INSPEC Abstract Number: B2000-06-2550F-130
Title: Integration issues for low dielectric constant materials in each generation of ULSI's
Author(s): Gomi, H.; Kishimoto, K.; Usami, T.; Koyanagi, K.; Yokoyama, T.; **Oda, N.**; Matsubara, Y.
Author Affiliation: ULSI Device Dev. Labs., NEC Corp., Kanagawa, Japan
Conference Title: Advanced Interconnects and Contacts. Symposium p. 509-19
Editor(s): Edelstein, D.C.; Kikkawa, T.; Ozturk, M.C.; Tu, K.-N.; Weitzman, E.J.
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 1999 Country of Publication: USA xiv+977 pp.
ISBN: 1 55899 471 8 Material Identity Number: XX-1999-03234
Conference Title: Advanced Interconnects and Contacts. Symposium
Conference Date: 5-7 April 1999 Conference Location: San Francisco, CA, USA
Language: English
Abstract: Technologies utilizing fluorinated silicon oxide (FSG, k=3.6) and hydrogen silsesquioxane (HSQ, k=3.0) have been established for 0.25 mu m and 0.18 mu m generation ULSIs. However, low-k materials for the next generation ULSIs, which have a dielectric constant of less than 3.0, have not yet become mature. In this paper, we review process integration issues in applying FSG and HSQ, and describe integration results and device performance using fluorinated amorphous carbon (a-C:F, k=2.5) as one of the promising low-k materials for next generation ULSIs.
Subfile: B

23/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5545768 INSPEC Abstract Number: B9705-2550F-051
Title: Barrier metal free copper damascene interconnection technology using atmospheric copper reflow and nitrogen doping in **SiOF** film
Author(s): Mikagi, K.; Ishikawa, H.; Usami, T.; Suzuki, M.; Inoue, K.; **Oda, N.**; Chikaki, S.; Sakai, I.; Kikkawa, T.
Author Affiliation: ULSI Device Dev. Lab., NEC Corp., Kanagawa, Japan
Conference Title: International Electron Devices Meeting. Technical Digest (Cat. No.96CH35961) p.365-8
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA 960 pp.
ISBN: 0 7803 3393 4 Material Identity Number: XX97-00080
U.S. Copyright Clearance Center Code: 0 7803 3393 4/96/$5.00
Conference Title: International Electron Devices Meeting. Technical Digest
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 8-11 Dec. 1996 Conference Location: San Francisco, CA, USA
Language: English

Abstract: This paper describes a barrier metal free copper damascene interconnection technology using atmospheric copper reflow and nitrogen doping in **SiOF** films for improvement of RC delay. Formation of a thin barrier layer for copper on the surface of **SiOF** film was achieved by NH/sub 3/ plasma treatment. Barrier metal free copper damascene interconnects having a resistivity of 1.8+or-0.03 mu Omega .cm, lower than that of Cu/TiN structures, were successfully fabricated without peeling-off failures. By use of this structure, a 25% reduction for Tpd in a 0.18 mu m CMOS technology, compared with that of the Cu/TiN structure, was confirmed by SPICE simulation.
Subfile: B

23/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04624831
E.I. No: EIP97023516125
Title: Barrier metal free copper damascene interconnection technology using atmospheric copper reflow and nitrogen doping in **SiOF** film
Author: Mikagi, K.; Ishikawa, H.; Usami, T.; Suzuki, M.; Inoue, K.; **Oda, N.**; Chikaki, S.; Sakai, I.; Kikkawa, T.
Corporate Source: NEC Corp, Kanagawa, Jpn
Conference Title: Proceedings of the 1996 IEEE International Electron Devices Meeting
Conference Location: San Francisco, CA, USA Conference Date: 19961208-19961211
E.I. Conference No.: 46059
Source: Technical Digest - International Electron Devices Meeting 1996. IEEE, Piscataway, NJ, USA,96CH35961. p 365-368
Publication Year: 1996
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: This paper describes a barrier metal free copper damascene interconnection technology using atmospheric copper reflow and nitrogen doping in **SiOF** film for improvement of RC delay. Formation of a thin barrier layer for copper on the surface of **SiOF** film was achieved by NH//3 plasma treatment. Barrier metal free copper damascene interconnects having 1.8 plus or minus 0.03 mu Omega center dot cm in a resistivity, which was lower than that of Cu/TiN structure, were successfully fabricated without peeling-off failures. By use of this structure, 25% reduction for Tpd in a 0.18 mu m CMOS, compared with Cu/TiN structure, was confirmed by SPICE simulation. (Author abstract) 3 Refs.

14/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7102780 INSPEC Abstract Number: A2002-01-7865P-011, B2002-01-2810-008
Title: Infrared spectroscopy study of low-dielectric-constant fluorine-incorporated and carbon-incorporated silicon **oxide** **films**
Author(s): Yoon-Hae Kim; Moo Sung Hwang; Hyeong Joon Kim; Jin Yong Kim; Young Lee
Author Affiliation: Sch. of Mater. Sci. & Eng., Seoul Nat. Univ., South Korea
Journal: Journal of Applied Physics vol.90, no.7 p.3367-70
Publisher: AIP,
Publication Date: 1 Oct. 2001 Country of Publication: USA
CODEN: JAPIAU ISSN: 0021-8979
SICI: 0021-8979(20011001)90:7L.3367:ISSD;1-V
Material Identity Number: J004-2001-020
U.S. Copyright Clearance Center Code: 0021-8979/2001/90(7)/3367(4)/$18.00
Language: English
Abstract: Bonding characteristics of low-dielectric-constant (low-k) fluorine-incorporated silicon oxide (**SiOF**) and carbon-incorporated silicon **oxide** (SiOC) **films** prepared by plasma enhanced chemical vapor deposition were investigated by Fourier transform infrared spectroscopy (FTIR). The frequency of Si-O stretching vibration mode in **SiOF** film shifted to higher wave number (blueshift) with the increase of fluorine incorporation, while that in SiOC film shifted to lower wave number (redshift) as the carbon content increased. In N/sub 2/-annealed SiOC film, the Si-O stretching frequency slightly shifted to lower wave number. To elucidate these phenomena, we have developed the "bonding structure model" based on the electronegativity of an atom. The frequency shifts observed in the FTIR spectra of **SiOF** and SiOC films were well explained by this model.

14/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6439764 INSPEC Abstract Number: B2000-01-2550F-061
Title: A manufacturable and reliable low-k inter-metal dielectric using fluorinated oxide (FSG)
Author(s): Chang, W.; Jang, S.M.; Yu, C.H.; Sun, S.C.; Liang, M.S.
Author Affiliation: Res. & Dev., Taiwan Semicond. Manuf. Co., Hsin-Chu, Taiwan
Conference Title: Proceedings of the IEEE 1999 International Interconnect Technology Conference (Cat. No.99EX247) p.131-3
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA 295 pp.
ISBN: 0 7803 5174 6 Material Identity Number: XX-1999-01750
U.S. Copyright Clearance Center Code: 0 7803 5174 6/99/$10.00
Conference Title: Proceedings of the IEEE 1999 International Interconnect Technology Conference
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 24-26 May 1999 Conference Location: San Francisco, CA, USA
Language: English
Abstract: A manufacturable and reliable low-k intermetal dielectric (IMD) using FSG is demonstrated. Film properties such as thickness, refractive index, stress and fluorine content and their thermal stability have been characterized. Dependency of **line**-to-**line** capacitance, via contact resistance (R/sub c/), and hot carrier reliability on FSG based IMD schemes are compared. We conclude that a simple, full FSG IMD with lower F content (4.7%) without undoped oxide (USG) as under- or cap-layer is feasible to achieve best interconnect performance with excellent thermal stability. Various product reliability tests demonstrate that the FSG IMD is highly reliable.

14/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5928598 INSPEC Abstract Number: B9807-1265D-012
Title: A 0.7- mu m-pitch double level Al interconnection technology for 1-Gbit DRAMs using SiO/sub 2/ mask Al etching and plasma enhanced chemical vapor deposition **SiOF**
Author(s): Yokoyama, T.; Yamada, Y.; Kishimoto, K.; Usami, T.; Kawamoto, H.; Ueno, K.; Gomi, H.
Author Affiliation: ULSI Device Dev. Lab., NEC Corp., Sagamihara, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes Rev. Pap. (Japan) vol.37, no.3B p.1140-4
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: March 1998 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199803)37:3BL.1140:PDLI;1-X
Material Identity Number: F221-98006
Conference Title: Solid State Devices and Materials
Conference Date: 16-19 Sept. 1997) Conference Location: Hamamatsu, Japan
Language: English
Abstract: A 0.7- mu m-pitch double level aluminum (Al) interconnection technology on a 1- mu m-high step is established for 1-Gbit dynamic random access memories (DRAMs). A SiO/sub 2/ film which has a high resistance to Al etching was used as the mask layer. 0.35- mu m-width Al wirings were fabricated even on a 1- mu m-high step. 0.2- mu m-spaces (aspect ratio=2.5) between the taper shaped Al **lines** were filled, for the first time, by a plasma enhanced chemical vapor deposition (PECVD) fluorine doped silicon **oxide** (**SiOF**) **film** (epsilon =3.9). The **SiOF** film capped with the PECVD SiO/sub 2/ film has enough stability for the process integration. It was confirmed that these technologies can be applied to a double level Al interconnection using a 0.3- mu m-diameter tungsten (W) plug.

14/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5863250 INSPEC Abstract Number: B9804-2550F-078
Title: The integration of interlayer dielectric deposition and chemical mechanical polishing
Author(s): McAfee, A.; Koos, D.A.; McArdle, S.; Jacobs, M.; Hiatt, R.
Author Affiliation: New Technol. Group, Motorola Inc., Mesa, AZ, USA
Conference Title: Science and Technology of Semiconductor Surface Preparation. Symposium p.109-14
Editor(s): Higashi, G.S.; Hirose, M.; Raghavan, S.; Verhaverbeke, S.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1997 Country of Publication: USA xii+540 pp.
ISBN: 1 55899 381 9 Material Identity Number: XX97-03043
Conference Title: Science and Technology of Semiconductor Surface Preparation. Symposium
Conference Date: 1-3 April 1997 Conference Location: San Francisco, CA, USA
Language: English
Abstract: This paper addresses an important process issue in the integration of chemical mechanical polishing (CMP) with interlayer dielectric (ILD) deposition for advanced back end processing. **Gap** fill between metal **lines** is achieved by using a dep-etch-dep technique for the tetraethylorthosilicate (TEOS) ILD deposition. The ILD layer is then planarized by CMP. Vias are etched through the ILD and filled with tungsten plugs in a blanket tungsten deposition and tungsten CMP sequence. Delamination has been observed at the interface between the TEOS layers following the blanket tungsten deposition and before or during tungsten CMP. The weak interface between the TEOS layers was found to be the result of residual carbon and fluorine from the tetrafluoromethane (CF4) doped etch process. The interface between the TEOS layers was examined using X-ray photoelectron spectroscopy (XPS) and atomic force microscopy (AFM). Experiments were carried out to determine if the residue and subsequent delamination could be eliminated by modifying the dep-etch-dep process. An improved process was identified and has been implemented on a 0.5 mu m CMOS and mixed-mode BiCMOS production line with no subsequent occurrence of interfacial delamination.
Subfile: B

14/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

5825089 INSPEC Abstract Number: B9803-2550F-041
Title: Integration of a stack of two fluorine doped silicon **oxide** thin **films** with interconnect metallization for a sub-0.35 mu m inter-metal dielectric application
Author(s): Baud, L.; Passemard, G.; Gobil, Y.; M'Saad, H.; Corte, A.; Pires, F.; Fugier, P.; Noel, P.; Rabinzohn, P.; Beinglass, I.
Author Affiliation: Appl. Mater., Meylan, France
Journal: Microelectronic Engineering Conference Title: Microelectron. Eng. (Netherlands) vol.37-38 p.261-9
Publisher: Elsevier,
Publication Date: Nov. 1997 Country of Publication: Netherlands
CODEN: MIENEF ISSN: 0167-9317
SICI: 0167-9317(199711)37/38L.261:ISFD;1-A
Material Identity Number: F621-97006
U.S. Copyright Clearance Center Code: 0167-9317/97/$17.00
Conference Title: Second European Workshop on Materials for Advanced Metallization. MAM'97
Conference Sponsor: Int. Union for Vacuum Sci., Tech. & Applications; Minist. Educ. Nat. Enseignement Superieur
Conference Date: 16-19 March 1997 Conference Location: Villard de Lans, France
Language: English
Abstract: Fluorine doped silicon **oxide films** were deposited using an HDP-CVD system and a PECVD system to realize a stack for integration into a metal **line** architecture. The moisture absorption resistance of both films was investigated by film exposure to a humid atmosphere for 1 week followed by annealing. The physical properties of uncapped FSG films were measured before and after testing in a humid atmosphere and after outgassing. Moisture absorption increases with the fluorine content for both films, and this moisture absorption creates fluorine desorption, clearly visible after outgassing, for concentrations above 6%at. fluorine. The mechanical stress, density and refractive index were also measured to follow the stability evolution. A very stable process was confirmed for both FSG HDP and PECVD layers for a **fluorine concentration** less than 6%at. Finally, the capability of reaching a dielectric constant of 3.5+or-0.05 for FSG HDP-CVD films was shown. In a second step, integration was evaluated. No problem occurs for chemical mechanical polishing of FSG films, via etching, metal barrier adhesion and W plug metallization, leading to a partial integrated structure. These results are very promising for the integration of FSG films as intermetal dielectrics for devices.

14/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5362062 INSPEC Abstract Number: A9619-6855-094
Title: Instability of Si-F bonds in fluorinated silicon **oxide** (**SiOF**) **films** formed by various techniques
Author(s): Homma, T.
Author Affiliation: ULSI Device Dev. Labs., NEC Corp., Kanagawa, Japan
Journal: Thin Solid Films vol.278, no.1-2 p.28-31
Publisher: Elsevier,
Publication Date: 15 May 1996 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
SICI: 0040-6090(19960515)278:1/2L.28:IBFS;1-K
Material Identity Number: T070-96014
U.S. Copyright Clearance Center Code: 0040-6090/96/$15.00
Language: English
Abstract: Instability of Si-F bonds in fluorinated silicon **oxide** (**SiOF**) **films** is studied. Al **wiring** corrosion and underlayer SiO/sub 2/ etching problems are the major issues for the use of **SiOF** interlayer dielectric films. To clarify the mechanism, three kinds of **SiOF** films have been used for this study. They are: (i) a fluorinated silicon **oxide** (**SiOF**) **film** prepared by room-temperature chemical vapour deposition (RTCVD) using fluorotriethoxysilane and pure water as gas sources; (ii) a fluorinated spin-on-glass (SOG) film prepared by fluorotrialkoxysilane vapor treatment (FAST); and (iii) a room-temperature liquid phase deposition (LPD) **SiOF** film. The initial refractive indices for the RTCVD-**SiOF**, FAST-SOG and LPD-**SiOF** films are 1.400, 1.398 and 1.433, respectively. After conducting a pressure cooker test (PCT) at 125 degrees C for 520 h, the refractive indices for the RTCVD-**SiOF**, FAST-SOG and LPD-**SiOF** films increase to 1.450, 1.440 and 1.436, respectively. The Si-O bond peak absorption coefficient for the LPD-**SiOF** film decreases at the early stage of PCT, but those for the RTCVD-**SiOF** and FAST-SOG films increase at the early stage of PCT. The initial Si-F bond peak absorption coefficient for the RTCVD-**SiOF** film is much higher than those for the LPD-**SiOF** and FAST-SOG films.

14/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

5240013 INSPEC Abstract Number: B9605-0520F-087
Title: Properties of fluorinated silicon **oxide films** formed using fluorotriethoxysilane for interlayer dielectrics in multilevel interconnections
Author(s): Homma, T.
Author Affiliation: ULSI Device Dev. Lab., NEC Corp., Sagamihara, Japan
Journal: Journal of the Electrochemical Society vol.143, no.3 p. 1084-7
Publisher: Electrochem. Soc,
Publication Date: March 1996 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
SICI: 0013-4651(199603)143:3L.1084:PFSO;1-C
Material Identity Number: J010-96003
U.S. Copyright Clearance Center Code: 0013-4651/96/$7.00
Language: English
Abstract: Properties of a fluorinated silicon **oxide** (**SiOF**) **film** for interlayer dielectrics in multilevel interconnections of ultralarge-scale integrated circuits (ULSIs) are investigated. The **SiOF** films are formed by a room temperature chemical vapor deposition (RTCVD) technique using fluorotriethoxysilane [FSi(OC/sub 2/H/sub 5/)/sub 3/, FTES] and pure water as gas sources. The **SiOF** film property changes by annealing at 400 or 900 degrees C are studied. Although the Si-O bond absorption peak position in the Fourier transform infrared (FTIR) spectrum is not changed by 400 degrees C annealing, the peak position for the 900 degrees C annealed **SiOF** films shifts to low wave numbers. The full width at half-maximum (FWHM) of the Si-O bond absorption peak increases by 400 degrees C annealing, and it further increases by 900 degrees C annealing. The tendency of the Si-F bond peak absorption coefficient change is inverse to the change of FWHM, indicating that fluorine influences the Si-O bond nature. Other properties such as the **fluorine** atomic **concentration**, refractive index, etching rate, shrinkage, residual stress, and leakage current density are changed by the annealing. These property changes are due to changes in the chemical bonding structure. No crack is observed for the **SiOF** films formed on aluminum **wiring** patterns after 400 degrees C annealing.

14/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

5208855 INSPEC Abstract Number: A9608-8115H-012, B9604-0520F-110
Title: Characteristics of **SiOF** films formed using tetraethylorthosilicate and fluorotriethoxysilane at room temperature by chemical vapor deposition
Author(s): Homma, T.
Author Affiliation: ULSI Device Dev. Lab., NEC Corp., Sagamihara, Japan
Journal: Journal of the Electrochemical Society vol.143, no.2 p. 707-11
Publisher: Electrochem. Soc,
Publication Date: Feb. 1996 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
SICI: 0013-4651(199602)143:2L.707:CSFF;1-K
Material Identity Number: J010-96002
U.S. Copyright Clearance Center Code: 0013-4651/96/$7.00
Language: English
Abstract: The characteristics of **SiOF** films deposited using tetraethylorthosilicate (TEOS) and fluorotriethoxysilane [FTES: FSi(OC/sub 2/H/sub 5/)/sub 3/] at room temperature by chemical vapor deposition (RTCVD) have been studied. The RTCVD technique utilizes FTES, TEOS, and pure water as gas sources. The **SiOF** films are deposited by changing the FTES concentration in TEOS and FTES gas mixtures. The **SiOF** film deposition does not occur without the presence of FTES gas. The deposition rate increases with increasing the FTES concentration, then saturates at about 12 nm/min while the FTES concentration is 80%. The relationship between the film deposition rate and the FTES percentage in TEOS and FTES gas mixture is not linearly proportional. The deposited **SiOF** film properties such as refractive index, Si-O bond nature, residual OH content, etching rate (1:30 buffered hydrofluoric acid), and leakage current are almost independent of the FTES concentration in the range from 20 to 100%. Residual **fluorine concentrations** for the **SiOF** films deposited at the FTES concentrations of 20, 50, 80, and 100% are 1.91*10/sup 21/, 1.82*10/sup 21/, 1.51*10/sup 21/, and 1.51*10/sup 21/ atom/cm/sup 3/, respectively. The conformability of the **SiOF** films on Al **wiring** patterns is close to 100%. The formation mechanism of **SiOF** film is then described in a series of five chain reactions.

14/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

4405101 INSPEC Abstract Number: B9306-0520F-027
Title: A room temperature chemical vapor deposition **SiOF** film formation technology for the interlayer in submicron multilevel interconnections
Author(s): Homma, T.; Yamaguchi, R.; Murao, Y.
Author Affiliation: ULSI Device Dev. Labs., NEC Corp., Kanagawa, Japan
Journal: Journal of the Electrochemical Society vol.140, no.3 p. 687-92
Publication Date: March 1993 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
Language: English
Abstract: A new interlayer dielectric film formation technology for multilevel interconnection by catalytic chemical vapor deposition has been developed. This technique utilizes fluorotriethoxysilane (FSi(OC/sub 2/H/sub 5/)/sub 3/) and water vapor as gas source. The films deposited at 25 degrees C have remarkably good properties, such as tightly bonded Si-O networks with no OH radicals, large density value (2.20 g/cm/sup 3/), small residual stress (50 MPa), low leakage current, and small dielectric constant (3.7), although the film contains residual fluorine and carbon atoms with 5.3*10/sup 21/ and 2*10/sup 21/ atom/cm/sup 3/, respectively. Based on the film characterization results, the authors speculate that the reaction sequence for the film deposition is: hydrolysis of fluorotriethoxysilane monomers, formation of siloxane oligomers with reaction by-product (alcohol), adsorption of the oligomers to the wafer surface, and then polymerization. The electrical conduction mechanism study revealed that the Schottky emission was dominant for the electric conduction through the film. It also has clarified that the deposition film thickness has no dependence on Al **wiring** widths, and is completely isotropic with no crack or keyhole in the film.
Subfile: B

14/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

03971578 INSPEC Abstract Number: A91116663, B91062797
Title: Surface composition analysis of HF vapour cleaned silicon by X-ray photoelectron spectroscopy
Author(s): Ermolieff, A.; Martin, F.; Amouroux, A.; Marthon, S.; Westendorp, J.F.M.
Author Affiliation: CEA, Div. LETI/D.OPT, CENG, Grenoble, France
Journal: Applied Surface Science vol.48-49 p.178-84
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Conference Title: 5th International Conference on Solid Films and Surfaces. ICSFS-5
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Conference Date: 13-17 Aug. 1990 Conference Location: Providence, RI, USA
Language: English
Abstract: X-ray photoelectron spectroscopy (XPS) measurements on silicon surfaces treated by HF gaseous cleaning are described. Various cleaning recipes, which essentially differ by the amount of water present during the reaction were studied; the composition of the silicon surface was measured in terms of monolayer coverage of oxygen, fluorine and carbon. These gaseous cleaned surfaces are compared with those of commonly deglazed silicon samples by using an aqueous HF bath. The F(1s), O(1s), Si(2p), C(1s) photoelectron **lines** were monitored, and concentrations determined as usual by integration of the **lines** after removal of the nonlinear background. The F(1s), C(1s) and Si(2p) **lines** were decomposed into several components corresponding to different chemical bonds. The results show that the amount of fluorine is directly correlated with the amount of oxygen: the higher the oxygen level on the sample, the more important is the fluorine content till 0.7 ML, essentially in a O-Si-F bonding state. For more aggressive etching leaving less than one monolayer of oxygen, the Si-F bond becomes predominant. The ratio of the SiF to OSiF concentrations is a significant signature of the deoxidation state of the surface. Hydrophobicity of the wafer appears in the range of 25% Si-F bonds. With very aggressive etching processes, 67% Si-F bonds and 33% O-Si-F bonds are reached and the total amount of fluorine drops below 0.3 ML. For comparison, only Si-F bonds are observed after a wet etching in a dilute HF bath without a rinse with a much lower **fluorine concentration**. The balance between Si-F and O-Si-F remains stable and seems to be representative of the surface states provided by the etching process.

14/3,AB/11 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

04736591 Genuine Article#: UD941 Number of References: 11
Title: ELIMINATION OF AL **LINE** AND VIA RESISTANCE DEGRADATION UNDER HTS TEST IN APPLICATION OF F-DOPED OXIDE AS INTERMETAL DIELECTRIC (Abstract Available)
Author(s): HWANG BK; CHOI JH; LEE S; FUJIHARA K; CHUNG UI; LEE SI; LEE MY
Corporate Source: SAMSUNG ELECT CO LTD,SEMICOND RES & DEV CTR,SAN24,NONGSEO RI,KIHEUNG EUP/YONGIN KUN/KYUNGKI DO/SOUTH KOREA/
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1996, V35, N2B (FEB), P1588-1592
ISSN: 0021-4922
Language: ENGLISH Document Type: ARTICLE
Abstract: Fluorine-doped silicon oxide (**SiOF**) as intermetal dielectric (IMD) layer was deposited by conventional plasma-enhanced chemical vapor deposition (CVD). The main issues in the application of **SiOF** as IMD are as follows: (1) instability of film properties such as stress and refractive index during HTS test, (2) desorption of H2O and HF gases from **SiOF** film, (3) increase of **line** resistance, (4) wedgelike defects of metal **lines**, and (5) via resistance degradation during HTS test at 350 degrees C. The above problems in use of **SiOF** as IMD can be eliminated by the passivation of IMD with PE-SIN and the application of Ti underlayer before the second metal deposition.

14/3,AB/12 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03522589 JICST ACCESSION NUMBER: 98A0047838 FILE SEGMENT: JICST-E
'98 Latest semiconductor process technology. Technology & Equipment. Insulator forming technology. Insulator forming technology in the age of 300mm/0.18 .MU.m.
MATSUURA MASAZUMI (1); MASUKO YOJI (1)
(1) Mitsubishi Electr. Corp.
Gekkan Semiconductor World(Semiconductor World), 1997, VOL.16,NO.14, PAGE.273-278, FIG.7, TBL.1, REF.19
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes STI (shallow trench isolation) embedding technology, PMD (pre-metal dielectric) forming technology, and IMD (inter-metal dielectric) forming technology. In particular, **SiOF** film, HSQ (hydrogen silsesquioxane) film and organic materials are described for IMD.Improvement of a embedding performance is an essential problem for STI and PMD.It is necessary for IMD to select intercalation membrane structure and material appropriate for groove processing for Damascene **wiring**. CVD and Spin-on are used as film formation techniques, and inorganic and organic materials are used. Selection of suitable technologies is important for such film formation.

14/3,AB/13 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03431478 JICST ACCESSION NUMBER: 97A0823154 FILE SEGMENT: JICST-E
The Study on the Reaction Mechanism of HDP-**SiOF** Film and Inter-Metal-Dielectric Application.
SHIN H-J (1); KIM S-J (1); CHOI J-H (1); HWANG B-K (1); KANG H-K (1); LEE M-Y (1)
(1) Samsung Electronics Co., LTD., Kyungki-Do, KOR
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1997, VOL.97,NO.195(SDM97 43-67), PAGE.1-6, FIG.8, TBL.2, REF.4
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The fluorine-doped silicon oxide(**SiOF**) as a low dielectric material is formed by high density plasma(HDP) chemical vapor deposition(CVD) method using SiH4, SiF4, O2 and Ar as source gases. We studied the reaction mechanism of HDP-**SiOF** film formation, and evaluated the gap-fill characteristics and parasitic capacitance between metal **lines** for inter-metal dielectric(IMD) application. SiF4 gas is not only source of Si-F bond in **SiOF** film but also have in-situ chemically etching characteristics. In case of insufficient amount of O2 flux, the unstable Si-F2 bonds were formed in the HDP-**SiOF** film. The dielectric constant of HDP-**SiOF** film could be reduced by 23% compared to that of PE-TEOS **oxide film**. Using HDP-**SiOF** film as gap-filling material in IMD, the gap was completely filled at the aspec ratio below 2.0 and the parasitic capacitance between metal **lines** could be reduced by 15% compared to that of USG process. (author abst.

14/3,AB/14 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03197670 JICST ACCESSION NUMBER: 97A0709332 FILE SEGMENT: JICST-E
Characterization of **SiOF** Semiconductor Interlayer Insulator by Infrared Spectroscopy.
NAGAI NAOTO (1); YOSHIKAWA MASANOBU (1); ISHIDA HIDEYUKI (1); MATSUNOBE TAKASHI (1)
(1) Toray Research Center, Inc.
Handotai, Shuseki Kairo Gijutsu Shinpojiumu Koen Ronbunshu(Proceedings of the Symposium on Semiconductors and Integrated Circuits Technology), 1997, VOL.52nd, PAGE.56-61, FIG.18, TBL.1
JOURNAL NUMBER: F0108BAP
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: It is important in the low dielectric interlayer films to reduce the capacitance between metal **wires** in recent ultralarge scale integration(ULSI) device technologies to accomplish higher electric performance. Recently, many low dielectric constant materials have been proposed by several researchers. In particular, the most promising material is **SiOF** (fluorine doped SiO2 films), whose relative dielectric constant value is about 3.4. But the mechanism of lowering the k-value by fluorine doping is now under investigation. The other important problem is hygroscopic property of **SiOF** films. Infrared absorption spectroscopy is an useful technique to evaluate the chemical bonding structure, stress (or bond angle) and impurities such as Si-OH, Si-H and H2O in the **SiOF** films. In the present work, infrared spectroscopy has been applied to the investigation of structural change in various fluorine doping levels of **SiOF** films. It can be seen that not only Si-F bonds but also Si-F2 bonds are formed with increasing the fluorine content. The microstructure difference will be discussed between two preparation methods, TEOS(tetraethoxy silane)-CVD(chemical vapor deposition) and HDP(high density plasma)-CVD. The chemical bonding structure will be discussed compared to the results obtained by other spectroscopic techniques (Raman, Spectroscopic ellipsometry). In TEOS-CVD films, the decrease in refractive index from 1.46 to 1.44 (at 675nm) is correlated to the increase of Si-F bonds. On the other hand, the further decrease in refractive index seems to be related to the increase in S-F2 bonds. (author abst.)

14/3,AB/15 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03001071 JICST ACCESSION NUMBER: 96A0844101 FILE SEGMENT: JICST-E
Issues and Perspectives in Low-k Dielectric Technology and its Impact on Device Performance.
SHIBATA HIDEKI (1)
(1) Toshiba Purosesugiken
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1996, VOL.96,NO.226(SDM96 77-89), PAGE.45-50, FIG.11, TBL.1, REF.15
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A low dielectric constant ILD technology has become an issue of paramount importance in reducing interconnect capacitance for high performance and low power ULSIs. Use of **SiOF** can bring the relative dielectric constant(k) down to 3.3-3.7 and is in use in state-of-the-art 0.35 micron generation LSIs. Several organic materials such as parylene-F, N and F-doped PI have been reported for further k reduction(k=2-3). Moreover, recently, a gas-dielectric interconnect process which can potentially reduce k to almost the minimum physical value possible, 1.0 has been proposed. In this paper, several engineering issues and perspectives in various low-k schemes are presented, and its impact on improvement in device performance is discussed. (author abst.)

14/3,AB/16 (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02774794 JICST ACCESSION NUMBER: 96A0220316 FILE SEGMENT: JICST-E
The Troublesome Existence of Fluorine .EPSILON.3.5 **SiOF** Films. The Possibilities of Organic Films Intended for the 0.13.MU.m Era.
HASEGAWA TOSHIAKI (1); KADOMURA SHINGO (1); AOYAMA JUN'ICHI (1)
(1) Sony Corp.
Gekkan Semiconductor World(Semiconductor World), 1996, VOL.15,NO.2, PAGE.89-93, FIG.11, TBL.1, REF.6
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The dielectric constant is limited below 3.0 for **insulation film** between **layers** of the ULSI of 0.18.MU.m or less, and this paper evaluates the dielectric constant and heat-resistance of organic SOG and amorphous teflon for the material to make clear the limits. Simulation of **wiring** capacity depending on location of organic film shows that suppression of the electric field leaking above and below **wiring** is important for effective reduction in the **wiring** capacity. Remaining problems in the film quality include hardness, resistance to oxygen plasma, coefficient of thermal

expansion, and adhesiveness.

14/3,AB/17 (Item 6 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02774668 JICST ACCESSION NUMBER: 96A0200681 FILE SEGMENT: JICST-E
The Troublesome Existence of Fluorine .EPSILON.3.5 **SiOF** Films. CMP for **SiOF** Films-The Problem is Moisture Absorbancy.
MORIO MASASHI (1)
(1) Puresujanaru
Gekkan Semiconductor World(Semiconductor World), 1996, VOL.15,NO.2, PAGE.86-88, FIG.3, TBL.1, REF.2
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper explains problems (Si-F bonding and desorption of F in the film) of **SiOF** film in the film deposition process, and presents damage to **wiring** caused by hygroscopicity of the film in CMP.The damage is prevented by **SiOF** film as a barreir or without applying CMP directly but using **SiOF** film as a stopper layer. This paper summerizes each method and problems. Because of no conclusive solution for solving the trade-off between hygroscopicity and dielectric constant at present, applications of the CMP are limited.

14/3,AB/18 (Item 7 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02774667 JICST ACCESSION NUMBER: 96A0200680 FILE SEGMENT: JICST-E
The Troublesome Existence of Fluorine .EPSILON.3.5 **SiOF** Films. The Existence of Fluorine Concerns Process Engineers.
MUROYAMA MASAKAZU (1); HAGA YUTAKA (1); SASAKI MASAYOSHI (1)
(1) Sony Corp.
Gekkan Semiconductor World(Semiconductor World), 1996, VOL.15,NO.2, PAGE.82-85, FIG.7, TBL.1, REF.11
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper presents a method and conditions for preparing **SiOF** film by helicon-wave plasma CVD technology, and examines problems. This paper evaluates dependency on **fluorine concentration** of an aging variation in the clean room of the dielectric constant of the **SiOF** film, temperature-increased desorption analysis of the **SiOF** film having 3.5 of dielectric constant, bonding condition of fluorine by infrared spectrophotometry, embedding characteristics, and resistance toward water-permeability and Al-**wiring** corrosion. Although the effects of fluoric acid on the CMP process seem little because the generation of fluoric acid is little, further examination is necessary. Deterioration of eparticles

under mass-production is a potential problem.

14/3,AB/19 (Item 8 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02774666 JICST ACCESSION NUMBER: 96A0200679 FILE SEGMENT: JICST-E
The Troublesome Existence of Fluorine .EPSILON.3.5 **SiOF** Films.
Equipment Development Until March, Process Development Until Summer.
MATSUSHITA SHINJI (1)
(1) Puresujanaru
Gekkan Semiconductor World(Semiconductor World), 1996, VOL.15,NO.2, PAGE.76-80, FIG.3
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper examines issues and solutions for .EPSILON.3.5SiOF thin-film deposition technology using parallel-plate plasma CVD equipment. The problems of gap-filling time, metal attacking and the generation of fluoric acid are solved by the sandwich structure for the insulation laeyr hbetween **wiring** to solve the problem of hygroscopicity in **SiOF** film..EPSILON. is around 3.5.Although the problem originating from film quality can be solved when the monolayer structrue is developed eventually, uncertainty in the congeniality between the **SiOF** film and the CMP process still remains.

14/3,AB/20 (Item 9 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02376027 JICST ACCESSION NUMBER: 95A0470953 FILE SEGMENT: JICST-E
MUMIC approves effect of **layer insulation film** and flat **SiOF** film on hygroscopicity.
HOKO HIROMASA (1)
(1) Fujitsu Miekojo
Gekkan Semiconductor World(Semiconductor World), 1995, VOL.14,NO.5, PAGE.33-36, TBL.6
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The first DUMIC (Dielectrics & CMP For ULSI Multilevel Interconnection Conference in Santa Clara, February 21 - 22) was held. This is an international conference on **layer insulation film** of multilayer **wiring** and flattening of the film. During the conference, including the poster session, there were 51 presentations on gap film, CMP,SOG process and others. The most noticeable subject was **SiOF** film with improved absorbency.

14/3,AB/21 (Item 10 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02356146 JICST ACCESSION NUMBER: 95A0591319 FILE SEGMENT: JICST-E
Preparation of **SiOF** films with low dielectric constant by ECR plasma CVD.
FUKADA TAKASHI (1); AKAHORI TAKASHI (1)
(1) Sumitomo Met. Ind. Ltd.
Handotai, Shuseki Kairo Gijutsu Shinpojiumu Koen Ronbunshu(Proceedings of the Symposium on Semiconductors and Integrated Circuits Technology), 1995, VOL.48th, PAGE.54-59, FIG.8, REF.6
JOURNAL NUMBER: F0108BAP
UNIVERSAL DECIMAL CLASSIFICATION: 539.23:54-31 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A formation technology of low dielectric constant film for multilevel interconnection of ultra large scale integrated device(ULSI) has been studied. **SiOF** films are deposited by using RF-biased ECR plasma CVD with SiF4, SiH4 and O2 as material gases. The relative dielectric constant can be controlled from 4.0 to 3.2 by controlling SiF4 gas flow ratio(SiF4/(SiF4+SiH4)). The **SiOF** film with low dielectric constant is obtained as a result of tight Si-F bonding formation. Both measurements of pressure cooker test(PCT) and thermal desorption spectroscopy(TDS) indicate that fluorine atoms are tightly bonded to silicon atoms. Further, the film has excellent electrical properties with lower leakage current and higher breakdown voltage those of SOG and TEOS-O3 films. Excellent planarization and sub half micron gap filling without voids are also accomplished. The **SiOF** film deposited by using RF-biased ECR plasma CVD has many advantages to use for ULSI. (author abst.)

14/3,AB/22 (Item 11 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02335834 JICST ACCESSION NUMBER: 95A0201235 FILE SEGMENT: JICST-E
Special issue : Will CMP be used in the second generation of 64M and after?Electron cyclotron resonance plasma CVD equipment. CN4000 of Sumitomo Metal.
FUKADA TAKUJI (1); AKAHORI TAKASHI (1); KENDO YASUHIRO (1)
(1) Sumitomo Met. Ind. Ltd.
Gekkan Semiconductor World(Semiconductor World), 1995, VOL.14,NO.2, PAGE.82-83, FIG.3
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes the composition of the electron cyclotron resonance plasma CVD equipment called CN4000 for inter-**layer insulation films**, examples of embedding the film into the gap between Al and Al with aspect ratio of 2.1, and the permeability resistance of the SiO2 formation film. This paper also describes the

inter-**layer insulation film** of low dieletcric constant of 3.0 which is **SiOF** film formed by cyclotron resonance plasma CVD using SiF4 and O2 gasses as raw materials. Equipment performance improvement proven by the in-house trial manufacture **line** is also mentioned.

14/3,AB/23 (Item 12 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02249369 JICST ACCESSION NUMBER: 95A0145444 FILE SEGMENT: JICST-E
An application of Low dielectric **SiOF** film on 0.35.MU.m CMOS.
IDA JIRO (1); OTOMO ATSUSHI (1); USAMI TAKASHI (1); YOSHIMARU MASAKI (1); SHIMOKAWA KIMIAKI (1); KITA AKIO (1); ONODA HIROSHI (1); INO MASAYOSHI (1)
(1) Okidenkikogyo ChoLSIkenkaise
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1994, VOL.94,NO.409(ICD94 166-174), PAGE.35-40, FIG.12, TBL.1, REF.9
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The impact of a low dielectric film is demonstrated with a simple calculations. The low dielectric film Is effective on improving the propagation delay time in local routing and global routing. On the other hand, a low resistance material is effective only in global routing. The new low dielectric **SiOF** film has been applied on 0.35.MU.m CMOS and the deviation of the transistor parameter has been studied. The delay time improvement of 13% with loaded 2NAND has been obtained with the **SiOF** film applied. It is clearly indicated that the **SiOF** film is inevitable in 0.35.MU.m CMOS because the increase of **wiring** capacitance by the adjacent component makes the performance of 0.35.MU.m CMOS worse than that of 0.5.MU.m CMOS. (author abst.)

14/3,AB/24 (Item 13 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02237779 JICST ACCESSION NUMBER: 95A0040701 FILE SEGMENT: JICST-E
A Study of Film Structure in PECVD **SiOF**.
USAMI TAKASHI (1); SHIMOKAWA KIMIAKI (1); YOSHIMARU MASAKI (1)
(1) Oki Electr. Ind. Co., Ltd.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1994, VOL.94,NO.367(SDM94 140-156), PAGE.43-48, FIG.11, REF.8
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5 539.23:54-31
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Water absorption and desorption processes in PECVD fluorine-doped silicon oxide(**SiOF**) were studied using FT-IR and TDS. In **SiOF** film, Si-OH bonds and hydrofluoric acid were formed by hydrolysis reaction between Si-F bonds and absorbed water. The film natural structure and essential dielectric constant of **SiOF** films were also studied using P-SiN capped samples in order to get rid of effects of water absorption. It was clarified that Si-OH bonds are not existed in as deposited **SiOF** film and Si-F bonds has unknown some

states. And essential dielectric constant of **SiOF** film contained 14at.% fluorine was 2.8. This low dielectric constant was achevied by keeping off water absorption and hydrolysis reaction. (author abst.)

14/3,AB/25 (Item 14 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01983918 JICST ACCESSION NUMBER: 94A0037784 FILE SEGMENT: JICST-E
Special issue : **Wiring** materials and formation methods in next generation. Low dielectric constant **SiOF** film formation technology by the electron cyclotron resonance (ECR) plasma CVD method.
FUKADA TAKAFUMI (1); AKAHORI TAKASHI (1)
(1) Sumitomo Metal Industries, Ltd.
Gekkan Semiconductor World(Semiconductor World), 1993, VOL.12,NO.15, PAGE.170-173, FIG.10, REF.9
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2 621.3.049.75
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

14/3,AB/26 (Item 15 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01929368 JICST ACCESSION NUMBER: 94A0028466 FILE SEGMENT: JICST-E
Formation technology of Low Dielectric Constant **SiOF** Film Using C2F6 Additional PECVD System.
USAMI TAKASHI (1); SHIMOKAWA KIMIAKI (1); YOSHIMARU MASAKI (1)
(1) Oki Electric Industry Co., Ltd.
Handotai, Shuseki Kairo Gijutsu Shinpojiumu Koen Ronbunshu(Proceedings of the Symposium on Semiconductors and Integrated Circuits Technology), 1993, VOL.45th, PAGE.68-73, FIG.9, TBL.1, REF.13
JOURNAL NUMBER: F0108BAP
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A simple formation technology of new interlayer dielectric **film**, fluorine doped silicon **oxide** (**SiOF**), for multilevel interconnection of very large scale integration(VLSI) has been developed. This formation technique is hexafluoroethane (C2F6) addition to conventional tetraethoxysilane(TEOS) based plasma enhanced chemical vapor deposition(PECVD). The film contained Si-F bonds, and the **fluorine concentration** of the film was controlled by C2F6 flow rate. Furthermore Si-O bonds were influenced with Si-F bonds formation. Low dielectric constant caused by Si-F bond formation was obtained. The relative dielectric constant was 3.6 at 14 atomic% of the **fluorine concentration**. And essential gap-filling ability caused by in-situ etching by C2F6 plasma were also obtained. The film filled narrow gaps of 400nm width, perfectly. Therefore, this technology has very high capability for interlayer dielectric film formation of advanced VLSI devices. (author abst.)

14/3,AB/27 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

13707336 PASCAL No.: 98-0462060

A 0.7- mu m-pitch double level Al interconnection technology for 1-Gbit DRAMs using SiO SUB 2 mask Al etching and plasma enhanced chemical vapor deposition **SiOF**

YOKOYAMA Takashi; YAMADA Yoshiaki; KISHIMOTO Koji; USAMI Tatsuya; KAWAMOTO Hideaki; UENO Kazuyoshi; GOMI Hideki

ULSI Device Development Laboratories, NEC Corporation, 1120, Shimokuzawa, Sagamihara, Kanagawa 229-11, Japan; VLSI Manufacturing Engineering Division, NEC Corporation, 1120, Shimokuzawa, Sagamihara, Kanagawa 229-11, Japan

Journal: Japanese Journal of Applied Physics Part 2 : Letters, 1998-03, 37 (3B) 1140-1144

Language: English

A 0.7- mu m-pitch double level aluminum (Al) interconnection technology on a 1- mu m-high step is established for 1-Gbit dynamic random access memories (DRAMs). A SiO SUB 2 film which has a high resistance to Al etching was used as the mask layer. 0.35- mu m-width Al wirings were fabricated even on a 1- mu m-high step. 0.2- mu m-spaces (aspect ratio=2.5) between the taper shaped Al **lines** were filled, for the first time, by a plasma enhanced chemical vapor deposition (PECVD) fluorine doped silicon **oxide** (**SiOF**) **film** (<varepsilon>=3.9). The **SiOF** film capped with the PECVD SiO SUB 2 film has enough stability for the process integration. It was confirmed that these technologies can be applied to a double level Al interconnection using a 0.3- mu m-diameter tungsten (W) plug. (c) 1998 Publication Board, Japanese Journal of Applied Physics.

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E US5888905/PN
L2 1 S US5888905/PN
E JP07307293/PN
E JP09045769/PN
L3 1 S JP09045769/PN
E JP09139428/PN
L4 1 S JP09139428/PN
E JP10056009/PN
L5 1 S JP10056009/PN
E JP10022389/PN
L6 1 S JP10022389/PN
E JP7307293/PN
E JP07307293/PN

FILE 'HCAPLUS, WPIX, JAPIO' ENTERED AT 15:52:28 ON 03 JAN 2002

FILE 'DPCI' ENTERED AT 15:52:39 ON 03 JAN 2002
SET SMARTSELECT ON
L7 SEL PLU=ON L1 1- PN : 1 TERM
SET SMARTSELECT OFF

FILE 'HCAPLUS, WPIX, JAPIO' ENTERED AT 15:52:42 ON 03 JAN 2002
L8 2 S L7

FILE 'DPCI' ENTERED AT 15:52:53 ON 03 JAN 2002
SET SMARTSELECT ON
L9 SEL PLU=ON L2 1- PN : 1 TERM
SET SMARTSELECT OFF

FILE 'HCAPLUS, WPIX, JAPIO' ENTERED AT 15:52:56 ON 03 JAN 2002
L10 2 S L9

FILE 'DPCI' ENTERED AT 15:53:34 ON 03 JAN 2002
E US5106770/PN,PN.G,PN.D
L11 18 S (US5106770/PN OR US5106770/PN.G OR
US5106770/PN.D)
E US5888905/PN,PN.G,PN.D
L12 8 S (US5888905/PN OR US5888905/PN.G OR
US5888905/PN.D)
E JP07307293/PN,PN.G,PN.D
E JP0945769/PN,PN.G,PN.D
E JP09045769/PN,PN.G,PN.D
L13 1 S JP09045769/PN

E JP09139428/PN,PN.G,PN.D
L14 1 S JP09139428/PN
E JP10056009/PN,PN.G,PN.D
L15 2 S (JP10056009/PN OR JP10056009/PN.G OR JP10056009/PN.D)
E JP10022389/PN,PN.G,PN.D
L16 2 S (JP10022389/PN OR JP10022389/PN.G OR JP10022389/PN.D)

FILE 'DPCI, JAPIO, HCAPLUS' ENTERED AT 15:58:11 ON 03 JAN 2002
SET SMARTSELECT ON
L17 SEL PLU=ON L11 1- PN : 57 TERMS
SET SMARTSELECT OFF
L18 48 S L17
SET SMARTSELECT ON
L19 SEL PLU=ON L12 1- PN : 18 TERMS
SET SMARTSELECT OFF
L20 20 S L19
SET SMARTSELECT ON
L21 SEL PLU=ON L13 1- PN : 1 TERM
SET SMARTSELECT OFF
L22 3 S L21
SET SMARTSELECT ON
L23 SEL PLU=ON L14 1- PN : 1 TERM
SET SMARTSELECT OFF
L24 3 S L23
SET SMARTSELECT ON
L25 SEL PLU=ON L15 1- PN : 9 TERMS
SET SMARTSELECT OFF
L26 6 S L25
SET SMARTSELECT ON
L27 SEL PLU=ON L16 1- PN : 5 TERMS
SET SMARTSELECT OFF
L28 6 S L27
L29 77 S L18 OR L20 OR L22 OR L24 OR L26 OR L28

L30 4 S L29 AND ((DIFLUOROSILANONE) OR (SILICON (W) OXYFLUORIDE) OR (SILICON (W) FLUORIDE (W) OXIDE) OR (HEXAFLUORODISILOXANE) OR (OCTAFLUOROTRISILOXANE OR SIOF OR

L30 ANSWER 1 OF 4 JAPIO COPYRIGHT 2002 JPO
AN 1999-289012 JAPIO
TI SEMICONDUCTOR DEVICE AND ITS MANUFACTURE
IN ODA NORIAKI; IMAI KIYOTAKA
PA NEC CORP
PI **JP 11289012** A 19991019 Heisei
AI JP1998-091538 (JP10091538 Heisei) 19980403
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99
AB PROBLEM TO BE SOLVED: To obtain a semiconductor device in which a circuit operating speed does not become slow, whose power consumption is reduced and whose yield is enhanced by, a method wherein the fluorine concentration of an **SiOF** film in an interconnection interval part is made higher than the fluorine concentration of an **SiOF** film on an interconnection.
SOLUTION: A first-layer interconnection 8, a second-layer interconnection 15 and a third-layer interconnection 20 are formed sequentially from the lower part in such a way that they are composed of, e.g. barrier metal layers 5A, 5B, 5C composed of titanium in a film thickness of about 30 nm and titanium nitride in a film thickness of about 100 nm, aluminum films 6A, 6B, 6C in a film thickness of about 0.5 μm and titanium nitride films 7A, 7B, 7C in a film thickness of about 30 nm. In addition, low fluorine-concentration **SiOF** films 12, 17 have a fluorine concentration of less than 5 atomic %, and high fluorine-concentration **SiOF** films 11, 16 have a fluorine concentration of 5 atomic % or higher. In addition, plasma oxide films are formed between the low-fluorine-concentration **SiOF** film 12, the second-layer interconnection 15 as its upper-layer interconnection, the low-fluorine-concentration **SiOF** film 17 and the third-layer interconnection 20 as its upper-layer interconnection as to prevent corrosion from being generated due to the direct contact of the interconnections with fluorine.

L30 ANSWER 2 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:665500 HCAPLUS
DN 131:280230
TI Semiconductor device and fabrication thereof
IN Oda, Noriaki; Imai, Kiyotaka
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11289012	A2	19991019	JP 1998-91538	19980403 <--
	JP 3132557	B2	20010205		
	US 6274476	B1	20010814	US 1999-275532	19990324 <--
	CN 1231504	A	19991013	CN 1999-103534	19990402 <--
PRAI	JP 1998-91538	A	19980403		

AB The invention relates to a semiconductor device having multilevel interconnections, wherein the layout of **SiOF** interlayer dielec. films prevents delamination and minimizes capacitance between conductor layers.

L30 ANSWER 3 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:181214 HCAPLUS
DN 128:187483
TI Semiconductor device having fluorine-doped silicon oxide interlayer insulating films, and fabrication thereof
IN Usami, Tatsuya; Ishikawa, Hiraku
PA NEC Corporation, Japan
SO Brit. UK Pat. Appl., 33 pp.
CODEN: BAXXDU
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 2313954	A1	19971210	GB 1997-11575	19970603 <--
	GB 2313954	B2	20010725		
	US 6157083	A	20001205	US 1997-864388	19970528 <--
	JP 10056009	A2	19980224	JP 1997-145338	19970603 <--
	JP 3186998	B2	20010711		
	GB 2357902	B2	20010815	GB 2001-8233	19970603
PRAI	JP 1996-140003	A	19960603		
	GB 1997-11575	A3	19970603		

AB To prevent the increase of capacity between layers in a multilayer interconnection structure and to prevent increase of via hole resistance, a 1st fluorine-doped plasma SiO2 film having a relatively high F concn. is formed on metallic interconnections on a semiconductor substrate surface, and then a 2nd fluorine-doped plasma SiO2 film having a relatively low fluorine concn. is formed and flattened by chem. machine polishing, etc., so that it is not hygroscopic. SiO2 films may be formed beneath and above the films. Via holes may then be formed through the films to connect the interconnections with interconnections of another layer.

L30 ANSWER 4 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:244164 HCAPLUS
DN 126:232222
TI Semiconductor device and fabrication thereof
IN Nakasaki, Yasushi; Myajima, Hideshi
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09045769	A2	19970214	JP 1995-193901	19950728 <--

AB The invention relates to a semiconductor LSI, e.g., wherein the insulator film for the isolation structure consists of SiO2 contg. -SiF, -SiF2 and -SiF3 moieties.

SYSTEM:OS - DIALOG OneSearch
File 350:Derwent WPIX 1963-2001/UD,UM &UP=200176
(c) 2001 Derwent Info Ltd
*File 350: Price changes as of 1/1/02. Please see HELP RATES 350.

File 347:JAPIO OCT 1976-2001/Aug(UPDATED 011203)
(c) 2001 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run. See HELP NEWS 347 for details.

Set	Items	Description
S1	167	((DIFLUOROSILANONE) OR (SILICON (W) OXYFLUORIDE) OR (SILICON (W) FLUORIDE (W) OXIDE) OR (HEXAFLUORODISILOXANE) OR (OCTAFLUOROTRISILOXANE OR SIOF OR SI(W)OXYFLUORIDE))
S2	8171	(FLUORINE OR F)(2N)(CONCENTRAT? OR PERCENT? OR PPM OR CENT OR WT OR WEIGHT)
S3	1937223	WIRE OR WIRES OR WIRING OR LINE OR LINES OR LINING
S4	4371	(WIRE OR WIRES OR WIRING OR LINE OR LINES OR LINING)(3N)(GAP)
S5	376540	(INSULAT? OR OXIDE OR DIELETRIC) (3N) (FILM? ? OR LAYER? OR COAT????)
S6	1	S1 AND S4
S7	62	S1 AND S3
S8	4	S7 AND S2
S9	54	S7 AND S5
S10	55	S6 OR S8 OR S9

? T S10/3,AB/1-55

10/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014144045
WPI Acc No: 2001-628256/200173
XRAM Acc No: C01-187228
XRPX Acc No: N01-468539
Forming Damascene interconnection structure on semiconductor by applying low permittivity material to superposed layers of conductors to form cavities between conductors of lower layer
Patent Assignee: COMMISSARIAT ENERGIE ATOMIQUE (COMS); STMICROELECTRONICS SA (SGSA)
Inventor: BERRUYER P; DEMOLLIENS O; MORAND Y; TROUILLET Y; TROUILLER Y
Number of Countries: 021 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2803438	A1	20010706	FR 9916637	A	19991229	200173	B
WO 200150524	A1	20010712	WO 2000FR3713	A	20001228	200173	

Abstract (Basic): FR 2803438 A1
Abstract (Basic):
NOVELTY - Forming a Damascene interconnection structure on a semiconductor includes forming first spaced apart conductors and second conductors in respective **insulating layers**. All second **insulating layer** and some of the first **insulating layer** are and a low permittivity material deposited that does not go between the first conductors so cavities are left between the first conductors.
DETAILED DESCRIPTION - The **insulation layers** are of silicon **dioxide** or **silicon oxyfluoride**. **Insulating** interface **layers** of silicon nitride, silicon oxynitride or silicon carbide are laid down beneath the first conductors and between them and the second conductors. The upper interface **layer** and the second **insulating layer** are both removed fully.

10/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014047897
WPI Acc No: 2001-532110/200159
XRAM Acc No: C01-158621
XRPX Acc No: N01-395221
Semiconductor device has silicon **oxide film** containing fluorine formed on **wiring**, on whose upper surface another silicon **oxide film** is formed, continuously
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001085517	A	20010330	JP 99258230	A	19990913	200159	B

Abstract (Basic): JP 2001085517 A

Abstract (Basic):
NOVELTY - A **wiring** (13) is formed on the substrate (11). Silicon **oxide film** (15) containing fluorine is formed on both sides of the **wiring**. Another silicon **oxide film** (16) is formed on the upper surface of film (15), continuously.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for semiconductor device manufacturing method.
USE - None given.
ADVANTAGE - As silicon **oxide film** containing fluorine is formed on both sides of **wiring**, film debonding of **silicon oxyfluoride** film is suppressed and **wiring** with outstanding and high reliability is obtained.

10/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013796538
WPI Acc No: 2001-280749/200129
XRAM Acc No: C01-085190
XRPX Acc No: N01-200148
Formation of opening in dielectric interconnect layers in self-aligned manner uses material of low dielectric constant in second dielectric layer
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: CHENG J; ERB D M; WANG F
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6207577	B1	20010327	US 99238049	A	19990127	200129	B

Abstract (Basic): US 6207577 B1
Abstract (Basic):
NOVELTY - An opening in dielectric interconnect layers is formed in a self-aligned manner by using material having low dielectric constant (low k) in second dielectric layer. The material has different etch sensitivity than oxide dielectric material to at least one etchant chemistry.

10/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013677399
WPI Acc No: 2001-161612/200117
XRAM Acc No: C01-048396
XRPX Acc No: N01-117897
Wiring layer formation method for semiconductor device manufacture - involves forming **SiOF film** on **insulating film** followed by vent formation and deposition of metal for **wiring**
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000012539	A	20000114	JP 98169778	A	19980617	200117	B

Priority Applications (No Type Date): JP 98169778 A 19980617
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000012539	A		10	H01L-021/3205	

Abstract (Basic): JP 2000012539 A
NOVELTY - The **SiOF** film (102) is formed on substrate (101) followed by vent formation for **wiring**. The fluorine on vent area is removed from **SiOF** film followed by oxygen plasma treatment on surface of vent. Titanium (104) and copper (105) are deposited on the vent.
USE - For semiconductor device such as ULSI manufacture.
ADVANTAGE - The deposition of copper and titanium on vent area, reduces degradation of background film and prevents damages to **wiring** layer.

10/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013600055
WPI Acc No: 2001-084262/200110
XRAM Acc No: C01-024814
XRPX Acc No: N01-064495
Multilayer **wiring** structure for logic devices, has fluorine content silicon **oxide film**, silicon hydride or silicon nitride film and spacer film formed between pair of metal wirings
Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ); MITSUBISHI DENKI KK (MITQ)
Inventor: GOTO K; MATSUURA M
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000286262	A	20001013	JP 9987521	A	19990330	200110	B
US 6222256	B1	20010424	US 99359654	A	19990726	200125	
US 20010021557	A1	20010913	US 99359654	A	19990726	200155	
			US 2001785248	A	20010220		
			Div ex patent US 6222256				

Abstract (Basic): JP 2000286262 A
Abstract (Basic):
NOVELTY - A metal **wiring** layer (2) comprising fluorine content silicon **oxide film** (**SiOF**) (3) is formed on a substrate (1). A silicon hydride (Si-H) or silicon nitride (Si-N) binding film (6) and spacer film (4) are sequentially formed on the **SiOF** film. Another metal **wiring** (5) is formed on the spacer.

10/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013539119
WPI Acc No: 2001-023325/200103
XRAM Acc No: C01-007056
XRPX Acc No: N01-018127
Trench isolation structure for metal oxide semiconductor integrated circuit includes **oxide** liner, dielectric material **layer** with specified dielectric constant, and fill oxide
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: FULFORD H J; GARDNER M I; MAY C E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6140691	A	20001031	US 97994701	A	19971219	200103	B

Abstract (Basic): US 6140691 A
Abstract (Basic):
NOVELTY - A trench isolation structure (70) has a trench within a semiconductor substrate, an oxide liner upon sidewall surfaces and a base of the trench, a dielectric material layer with dielectric constant of 2-3.8 within the trench, and a fill oxide having a different composition than the dielectric material. The dielectric

material is interposed between the fill oxide and oxide liner.
USE - For metal oxide semiconductor integrated circuit.
ADVANTAGE - The structure reduces the capacitance between active areas, thus decreasing the lateral width of the isolation structure. The minimized size of the structure increases circuit integration density while maintaining isolation of the active areas, thus problems, e.g. current undesirably passing from a source/drain region (82) of one transistor (72) to another are less likely to be encountered. The oxide liner and fill oxide function as good diffusion barriers against migration of species from the dielectric material. There is no etchback step of the dielectric material required to make the upper surface of the material approximately level with the substrate.

10/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013399227
WPI Acc No: 2000-571165/200053
Related WPI Acc No: 2000-523628
XRAM Acc No: C00-170153
XRPX Acc No: N00-422492
High density integrated circuit for microprocessor and semiconductor memory devices, comprises silicon substrate structures bonded at respective metal interlevel **lines**
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: GARDNER M I; HAUSE F; KADOSH D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6097096	A	20000801	US 97890377	A	19970711	200053	B

Abstract (Basic): US 6097096 A
Abstract (Basic):
NOVELTY - A high density integrated circuit (100) comprises two silicon substrate structures (10, 50) bonded at respective metal interlevel **lines** (28) via low temperature metal attachment method. Both structures has semiconductor formations and metal interlevel **lines** disposed on their top surfaces.
DETAILED DESCRIPTION - A high density integrated circuit comprises two silicon substrate structures. Both of the structures have semiconductor formations and metal interlevel **lines** disposed on their top surfaces. Both of the structures contain a protective coating (70) which covers the metal interlevel **lines** and a planarized low-K dielectric (72) which is disposed between the metal interlevel **lines**. The metal interlevel **lines** have a melting point temperature of less than 500degreesC. The low-K dielectric has 2-3.8 dielectric K-value. The protective coating of the second structure is less than 400Angstrom thick. The structures are bonded to one another at their respective metal interlevel **lines**.

10/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013351689
WPI Acc No: 2000-523628/200047
Related WPI Acc No: 2000-571165
XRAM Acc No: C00-155372

XRPX Acc No: N00-387020
High density integrated circuit formation for microprocessors, involves forming dielectric layer with fluorine content materials having specific low dielectric constant between metal patterns and protective coating
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: GARDNER M I; HAUSE F; KADOSH D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6080640	A	20000627	US 97890377	A	19970711	200047	B
			US 9845324	A	19980320		

Abstract (Basic): US 6080640 A
Abstract (Basic):
NOVELTY - Metallic patterns (28,68) with melting temperature less than 500 degreesC are formed on the silicon substrates (50,52). Planarized low dielectric layers (32,72) with dielectric constant of 2.0-3.8 are formed between patterns and protective coating. The flowing content dielectric material is selected from fluorosilicate glass, **silicon oxyfluoride**, hydrogen silsesquioxane and fluoro polyimide.
DETAILED DESCRIPTION - The metallic patterns and protective **coating** comprising **oxide** and nitride **layers** are formed on the top surface of both silicon substrates comprising nitride layer. Then a low dielectric material selected from fluorosilicate glass, fluoro polysilicon, fluoro polyimide, hydrogen silsesquioxane, polyphenylquinoxaline, polyquinoline, methysilsesquioxane polymer with **fluorine concentration** of 3-20 atom percent is formed between the patterns and coating. Then both substrates are bonded relevant to metal patterns at temperature of 350-550 degreesC. The back side of substrate are planarized.

10/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013331352
WPI Acc No: 2000-503291/200045
XRAM Acc No: C01-001961
XRPX Acc No: N01-005458
Insulation film formation in semiconductor device manufacture, involves forming lower HSQ film having material with low dielectric constant by spin coating, on semiconductor substrate
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM S J; PARK H S; SHIN H J; KIM S; PARK H; SHIN H
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 99057679	A	19990715	KR 9777745	A	19971230	200045	B
JP 11204645	A	19990730	JP 98157853	A	19980605	200102	
US 6277764	B1	20010821	US 98224560	A	19981230	200150	

Abstract (Basic): JP 11204645 A
Abstract (Basic):
NOVELTY - The lower HSQ film having material with low dielectric constant is formed by spin coating, on surface of semiconductor substrate (10) formed with metallic **wiring** (12). The upper **SiOF** film (32) containing material with low dielectric constant is formed on HSQ film by high density plasma chemical vapor deposition

(PCVD) technique. The **SiOF** film is planarized by chemo mechanical polishing.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **insulation film**.

USE - For forming double **layered insulation film** on metallic **wiring** in manufacture of semiconductor integrated circuit device.

10/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013177547
WPI Acc No: 2000-349420/200030
XRAM Acc No: C00-106155
XRPX Acc No: N00-261774

Sealing semiconductor substrate involves depositing a material of greater dielectric constant over the other to cover a bond pad and a metal **line** and filling its **gap**

Patent Assignee: INTEL CORP (ITLC)
Inventor: BALAKRISHNAN S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6054376	A	20000425	US 971261	A	19971231	200030	B

Abstract (Basic): US 6054376 A
Abstract (Basic):

NOVELTY - A substrate is sealed by depositing first and second material on a substrate, with the second material having greater dielectric constant (DC) than the first. The second material having a lower DC material covers a bond **gap** and a metal **line** on the substrate.

10/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013113930
WPI Acc No: 2000-285801/200025
XRAM Acc No: C00-086471
XRPX Acc No: N00-215242

Wiring layer of semiconductor integrated circuit, has **insulating film** between **wiring layers** which contains fluorine formed on titanium silicide

Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000077415	A	20000314	JP 98248796	A	19980905	200025	B

Abstract (Basic): JP 2000077415 A
Abstract (Basic):

NOVELTY - Titanium silicide film (108) is formed on a portion of diffused layer (106). The titanium silicide surface is covered by titanium nitride **film** (109). **SiOF insulating film** between **wiring layers** which contain fluorine, is formed on titanium silicide.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **wiring** layer formation method.

USE - For gate electrode of transistor, in semiconductor integrated circuit.

ADVANTAGE - Since **SiOF insulating film** is formed on titanium silicide, reaction of fluorine is prevented. Hence combination of titanium silicide diffused **layer**, **wiring** and silicon **oxide film** are made possible. Therefore high speed semiconductor device with secured favorable **layer insulation** capability can be obtained.

10/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013037607
WPI Acc No: 2000-209459/200019
XRAM Acc No: C00-064873
XRPX Acc No: N00-156310
Aluminium **wiring** formation method in semiconductor device - involves forming crystal grains of aluminium metal layer by heat treatment after which silicon **oxide film** containing fluorine is formed
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11135503	A	19990521	JP 97294634	A	19971027	200019	B

Abstract (Basic): JP 11135503 A

NOVELTY - Aluminum **wiring** pattern (3) is formed over the silicon **oxide layer** (8). The crystal grains of aluminum metal layer is formed by heat treatment after which silicon **oxide film** (9) containing fluorine is formed.

USE - In semiconductor device e.g. semiconductor integrated circuit (IC).

ADVANTAGE - Achieves stable orientation of metal grains without getting suppressed by **SiOF** film. Prevents deterioration of electromigration resistance of the **wiring**, thereby improving reliability of the **wiring**. DESCRIPTION OF DRAWING(S) - The figure shows sectional view of aluminum **wiring** formation method. (3) Aluminum **wiring** pattern; (8) Silicon **oxide layer**; (9) Silicon **oxide film**.

10/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013037563
WPI Acc No: 2000-209415/200019
XRAM Acc No: C00-064834
XRPX Acc No: N00-156266
Multilayer interconnection structure of semiconductor device - has **SiOF** film formed between metal **wiring** and silicone nitride film, above which another SiO - 2 film is formed, with silicone nitride film having water diffusion suppression properties
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11111845	A	19990423	JP 97271134	A	19971003	200019	B

Abstract (Basic): JP 11111845 A

NOVELTY - A fluorine added silicon **oxide film** (31) separates the **wiring** layer (20) and the silicone nitride film (32), above which another SiO2 film (33) is formed, with relative dielectric constant higher than **SiOF** film (31), but lower than film (32). The silicone nitride film (32) has water or hydroxide ion diffusion suppression properties. DETAILED DESCRIPTION - An upper **wiring** layer (50) is formed on the upper **insulating film** (33). Plug material (41) is embedded in the hole, which is linked to **wiring** (20) and formed through the layers (31-33). An INDEPENDENT CLAIM is also included for semiconductor device manufacturing method.

USE - For semiconductor device.

ADVANTAGE - Spreading of impurities and penetration of water or hydroxide ion are prevented, thus improving reliability of semiconductor device. DESCRIPTION OF DRAWING(S) - The figure shows sectional view of multilayer **insulation film** interconnection structure. (20,50) **Wiring** layers; (31) **SiOF** film; (32) Silicone nitride film; (33) SiO2 film; (41) Plug material.

10/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012909460
WPI Acc No: 2000-081296/200007
XRAM Acc No: C00-023090
Formation of **insulating film** - for use in multi layered **wiring**
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11330062	A	19991130	JP 98128837	A	19980512	200007	B

Abstract (Basic): JP 11330062 A

NOVELTY - The formation of an **insulating film** comprises a process for forming an **insulating film** by applying the plazma chemical vapor accumulation process with the fluorine gas and an organic silicon compound. DETAILED DESCRIPTION - The formation of an **insulating film** comprises a process for forming an **insulating film** by applying the plazma chemical vapor accumulation process with the fluorine gas and an organic silicon compound represented by a general formula R1mSi(OR2)n; R1 = 1-4C hydrocarbon or aromatic hydrocarbon; R2 = 1-4C hydrocarbon.

USE - Effectively used for the **insulating film** of the multilayered **wiring** in an integrated circuit device.

ADVANTAGE - The CF bond can be effectively formed. The coating film is a fluorocarbon silicon **oxide film**, so that the increase of the dielectric constant caused by the humidity absorption which is found in a conventional **SiOF** film, can be prevented.

Dwg.0/0

10/3,AB/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012837001
WPI Acc No: 2000-008833/200001
XRAM Acc No: C00-001560
XRPX Acc No: N00-008062
Wiring layer for semiconductor device - has **layer insulation film** with **fluorine concentration** higher in **wiring** portion than on **wiring**
Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE)
Inventor: IMAI K; ODA N
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11289012	A	19991019	JP 9891538	A	19980403	200001	B
CN 1231504	A	19991013	CN 99103534	A	19990402	200008	
KR 99082907	A	19991125	KR 9911693	A	19990402	200055	
US 6274476	B1	20010814	US 99275532	A	19990324	200148	

Abstract (Basic): JP 11289012 A
NOVELTY - The **fluorine concentration** of **SiOF layer insulation films** (11,16) in the **wiring** portion are higher than **fluorine concentration** of **SiOF layer insulation films** (12,17) on **wiring**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of semiconductor device.
USE - For semiconductor device with multilayered interconnection structure using **SIOF** as **insulating film**.
ADVANTAGE - Reduces **wiring** capacity. Prevents debonding of an interlayer film on the **wiring**.
DESCRIPTION OF DRAWING - The figure shows the sectional view of semiconductor device. (11,12,16,17) **SiOF layer insulation films**.

10/3,AB/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012580675
WPI Acc No: 1999-386782/199933
XRAM Acc No: C99-114027
XRPX Acc No: N99-289695
Integrated semiconductor circuit, e.g. a DRAM, exhibits reduced leakage current
Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: KUNIKIYO T
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19833955	A1	19990708	DE 1033955	A	19980728	199933	B
JP 11186378	A	19990709	JP 97354918	A	19971224	199938	
CN 1221213	A	19990630	CN 98118562	A	19980903	199944	

Abstract (Basic): DE 19833955 A1

Abstract (Basic):
NOVELTY - An IC has fluoride-filled isolation trenches (2) for separating elements on a semiconductor substrate (1).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(i) an IC having a first **wiring** above a semiconductor substrate, a second **wiring** between the substrate and the first **wiring** and a prop which is provided on the substrate for supporting the first **wiring** and which is separate from the second **wiring**, the two wirings being isolated only by a gas which fills a layer interspace between the wirings;
(ii) a semiconductor device including a semiconductor substrate with stacked layers, a gate electrode and a curved sidewall spacer which covers the stacked layers and which is separated from the stacked layers by a cavity; and
(iii) a semiconductor device including a semiconductor substrate with a gate **insulation film**, a polysilicon **film** and a silicide film which has a cavity.

10/3,AB/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012310635
WPI Acc No: 1999-116741/199910
XRAM Acc No: C99-034263
XRPX Acc No: N99-086329
Semiconductor device - has second **SiOF** film which has dielectric constant equal to or lower than that of first **SiOF** film, is formed on first **SiOF** film
Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10340897	A	19981222	JP 97149154	A	19970606	199910	B

Abstract (Basic): JP 10340897 A
NOVELTY - The metal **wiring** (22) is formed on the main-surface side of a semiconductor substrate (21). A first **SiOF** film (13) is provided covering the metal **wiring**. A second **SiOF** film (14) which has dielectric constant equal to or lower than that of the first **SiOF** film, is formed on the **SiOF** film (13).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is provided for manufacturing method of semiconductor device.
USE - None given.
ADVANTAGE - Prevents etching damage of metal **wiring**, during film formation. Enables formation of low dielectric constant **insulating film**. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of semiconductor device. (13) First **SiOF** film; (14) Second **SiOF** film; (21) Semiconductor substrate; (22) Metal **wiring**.

10/3,AB/18 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012285738
WPI Acc No: 1999-091844/199908
XRAM Acc No: C99-027376

XRPX Acc No: N99-067789
Multilayered interconnection **wiring** structure manufacture for semiconductor device - involves forming **insulating** cap **film** containing hygroscopic low material, on polished **insulating film**
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10326829	A	19981208	JP 97134183	A	19970523	199908	B

Abstract (Basic): JP 10326829 A
The method involves covering a **wiring** formed on silicon substrate by a **SiOF** film (64) having dielectric constant of 3.5. An **insulating film** is formed on the **SiOF** film.
Then, the **insulating film** and **SiOF film** are polished and exposed. An **insulating** cap **film** (66) containing hygroscopic material, is formed on the polished **insulating film**.
ADVANTAGE - Prevents debonding of metal **film** from **layer insulation film** of low dielectric constant. Suppresses hygroscopic property of **SiOF** film for moisture proofs. Suppresses increase in dielectric constant of **SiOF** film

10/3,AB/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011951715
WPI Acc No: 1998-368625/199832
XRPX Acc No: N98-288602
Insulating film formation method e.g. for semiconductor device manufacture for LSI - involves forming **SiOF** film in contact with copper **wiring** pattern formed on substrate by performing vapour phase epitaxy using mixed gas which does not contain hydrogen
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10144792	A	19980529	JP 97172696	A	19970630	199832	B

Abstract (Basic): JP 10144792 A
The method involves performing vapour phase epitaxy on the surface of the substrate to form **SiOF** film (23) using a mixed gas. The mixed gas contains fluorine content compounds such as flouride of oxygen group element, fluoride of noble gas, fluoride thiocarbonyl, perfluridated thiocarbonyl, fluoride carbonyl and fluoride sulphur.
Hydrogen is not included in the mixed gas. The **SiOF** film is formed in contact with a copper **wiring** pattern (22) formed on the substrate.

10/3,AB/20 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011908681
WPI Acc No: 1998-325591/199829
XRAM Acc No: C98-100254
XRPX Acc No: N98-254704

Silicon **oxide film** formation for semiconductor integrated circuits - involves forming plasma by introducing predetermined gases into container in which magnetic field is generated and maintaining electron temperature of plasma to predetermined value

Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10074756	A	19980317	JP 96228036	A	19960829	199829	B
JP 3228143	B2	20011112	JP 96228036	A	19960829	200174	

Abstract (Basic): JP 10074756 A

The method involves generating a magnetic field in a film forming container (3) in which the semiconductor wafer (13) is placed. The magnetic field is generated by an electromagnet (4) and the microwave which is generated by a magnetron (1). SiH2F2 gas (7a), O2 gas (7b) and Ar gas (7c) are introduced into the film forming container. Due to the magnetic field in the container the gases are ionised and plasma is formed.

By increasing the supply of SiH2F2 gas and the pressure in the reaction container, the electron temperature of the plasma is brought to 10eV or less, to reduce the increase in electron temperature of the SiF2 radical in the plasma. An **SiOF** film is formed on the surface of the semiconductor wafer.

ADVANTAGE - Provides low dielectric constant to **SiOF** film. Forms **SiOF** film which has low hygroscopic property and chemical reactivity. Forms **SiOF** film with high dielectric breakdown electric field. Restrains corrosion of semiconductor surface. Enables production of semiconductor device which reduces **wiring** delay.

Dwg.1/6

10/3,AB/21 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011768650
WPI Acc No: 1998-185560/199817
XRAM Acc No: C98-059069
XRPX Acc No: N98-147403
Wiring layer formation method for semiconductor device manufacture - involves forming **wiring** groove on low dielectric constant film which is deposited on first silicon **oxide film**
Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE)
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10041385	A	19980213	JP 96190657	A	19960719	199817	B
KR 98012612	A	19980430	KR 9734240	A	19970722	199917	
KR 258044	B1	20000601	KR 9734240	A	19970719	200130	

Abstract (Basic): JP 10041385 A
The method involves forming a first silicon **oxide film** (11) on the element area or **wiring** layer of a substrate (10). A low dielectric constant film such as a **SiOF** film (12) is deposited on the first silicon **oxide film**.
The **SiOF** film has a higher etching rate than the silicon **oxide film**. A **wiring** groove (13) is formed on the low dielectric constant film by anisotropic dry etching. A **wiring** metal is deposited on the whole surface containing the groove. Metals portions other than groove are removed by chemical mechanical polishing.
ADVANTAGE - Simplifies formation of groove **wiring**. Reduces **wiring** parasitic capacitance. Facilitates formation of implanting **wiring**.

10/3,AB/22 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011700174
WPI Acc No: 1998-117084/199811
XRAM Acc No: C98-038601
XRPX Acc No: N98-093996
Semiconductor device e.g. LSI - has fine particles added to **insulating film** to maintain dielectric constant
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10004087	A	19980106	JP 96154658	A	19960614	199811	B

Abstract (Basic): JP 10004087 A
The semiconductor device has a first **insulating film** (4) to cover a **wiring** pattern (3) formed over a SiO2 film (2) of Al system on silicon substrate (1). Fine particles consisting one from **SiOF**, SiOBN, SiBN, BN are added to the **insulating film** of low dielectric constant in resin.
ADVANTAGE - Offers reliable insulation. Improves operating speed.

Reduces power consumption.
Dwg.1/4

10/3,AB/23 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011589281
WPI Acc No: 1998-006410/199801
XRAM Acc No: C98-002252
XRPX Acc No: N98-005248
Plasma CVD of **insulator layer** in semiconductor device - involves reacting fluorinated silane to generate helicon wave plasma and depositing on surface oxidised silicon substrate
Patent Assignee: CANON HANBAI KK (CANO-N); HANDOTAI PROCESS KENKYUSHO KK (HAND-N)
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9275103	A	19971021	JP 9683728	A	19960405	199801	B
JP 2991657	B2	19991220	JP 9683728	A	19960405	200005	

Abstract (Basic): JP 9275103 A
The CVD involves reacting an organic compound of Si-F bond like trimethyl fluorosilane or triethyl fluorosilane with an oxygen-containing gas like nitrogen monoxide or oxygen to generate helicon wave plasma. An **SiOF** film is deposited on a surface-oxidised silicon substrate having **wiring** patterns of striped mesa formed on its surface in a CVD chamber.

10/3,AB/24 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011400614
WPI Acc No: 1997-378521/199735
XRAM Acc No: C97-121701
XRPX Acc No: N97-314705
Semiconductor device mfr, ,e.g. for LSI - involves forming **insulating film** containing **silicon oxyfluoride** over processed substrate, by CVD process using thiocarbonyl fluoride, silane and oxidising gas mixture
Patent Assignee: SONY CORP (SONY)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9162184	A	19970620	JP 95319048	A	19951207	199735	B

Abstract (Basic): JP 9162184 A
The method involves forming an interlayer **insulating film** (4) containing **SiOF** over a processed substrate (11) by CVD process. The process is carried out using a mixture of thiocarbonyl fluorides, silanes and oxidising gas.
An ultrasonic wave is applied to the processed substrate. The inner SiO2 layer receives equally the fluorine gas generated by decomposition of thiocarbonyl fluoride. The carbonyl residue formed is oxidised and removed out of the CVD chamber.
ADVANTAGE - The method avoids contamination, as carbonyl residue is removed; enables reliable semiconductor mfr, without any signal delay

by **wiring** layer; and improves integration density of memory.

10/3,AB/25 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011031393
WPI Acc No: 1997-009317/199701
XRAM Acc No: C97-002355
XRPX Acc No: N97-008515
Fluororesin system **insulating film** formation method for semiconductor IC device - involves forming carbon fluoride layer on surface of silicon substrate by exposing carbon film on substrate to fluoride environment
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8279500	A	19961022	JP 9578640	A	19950404	199701	B

Abstract (Basic): JP 8279500 A
The method involves forming a carbon film (2) on surface of a silicon substrate (1) which is then exposed in a fluoride environment (3).
The carbon film is thus converted into a carbon fluoride layer (4).
ADVANTAGE - Improved heat proof nature. Reduced relative permittivity when compared to **SiOF** film. Signal delay due to parasitic capacitance of **wiring** is avoided. Speed of device is improved.
Dwg.1/6

10/3,AB/26 (Item 26 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010470803
WPI Acc No: 1995-372157/199548
XRAM Acc No: C95-161465
XRPX Acc No: N95-274283
Semiconductor device prepn. with stable permittivity - by laminating silicon **oxide film** contg. fluorine on substrate by PCVD using high and low frequency alternate electric field
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7254592	A	19951003	JP 9445920	A	19940316	199548	B

Priority Applications (No Type Date): JP 9445920 A 19940316
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7254592	A		8	H01L-021/31	

Abstract (Basic): JP 7254592 A
A silicon **oxide film** contg. F is laminated on a substrate by plasma CVD under excitation of reaction gas using high frequency and low frequency electric field simultaneously.
USE - The method is suitable for forming **insulating film** of multilayer **wiring**.

ADVANTAGE - A **SiOF** film is produced with stable permittivity at normal air atmos.

10/3,AB/27 (Item 27 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010202130
WPI Acc No: 1995-103384/199514
XRAM Acc No: C95-047649
XRPX Acc No: N95-081495
Semiconductor element mfg. method - uses plasma CVD technique to form alternative layers of P-silica film and **silicon oxyfluoride** film over substrate by introducing respective gases
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7029975	A	19950131	JP 93170274	A	19930709	199514	B

Abstract (Basic): JP 7029975 A

The mfg. method uses a plasma CVD technique for the formation of inter-**layer insulating films** over a semiconductor substrate (11). A P-SiO2 **insulating film** (12) is formed over this substrate by introducing a gas. After forming this layer, the gas flow is stopped. Then a source gas is allowed to flow to form a SiOxFy **insulating film** (13) over this P-SiO2 film. After forming this layer, the corresponding gas flow is stopped. This process is repeated to form two more sets of alternative **layers**. Totally six **insulation layers** are formed over the substrate.

ADVANTAGE - Gives low level relative permittivity. Gives hydroscopic low **insulating film**. Increases lifetime by avoiding metal **wiring** corrosion problem of transistor

10/3,AB/28 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06858015
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 2001-085517 [JP 2001085517 A]
PUBLISHED: March 30, 2001 (20010330)
INVENTOR(s): ENOMOTO YASUYUKI
APPLICANT(s): SONY CORP
APPL. NO.: 11-258230 [JP 99258230]
FILED: September 13, 1999 (19990913)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **wiring** structure of high reliability, which is superior in adhesion by restraining exfoliation of an **SiOF**-(silicon **oxide**) **film**, in a **wiring** structure using an **SiOF** film having low permitivity.

SOLUTION: This semiconductor device is provided with a substrate 11, a **wiring** 13 which is formed on the substrate 11 and has a P-SiN film 14 formed on the upper surface, a silicon **oxide film** a 15 which is formed on the side part of the **wiring** 13 (includes the P-SiN film 14) and contains fluorine, a silicon **oxide film** 16, which is formed continuously on the P-SiN film 14 and the silicon **oxide film** 15 containing fluorine.

10/3,AB/29 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06808359
MANUFACTURE OF SEMICONDUCTOR DEVICE AND METHOD FOR FORMATION OF **INSULATING FILM**

PUB. NO.: 2001-035844 [JP 2001035844 A]
PUBLISHED: February 09, 2001 (20010209)
INVENTOR(s): ENOMOTO YASUYUKI
APPLICANT(s): SONY CORP
APPL. NO.: 11-204635 [JP 99204635]
FILED: July 19, 1999 (19990719)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent the delamination of an **insulating film**.

SOLUTION: **Wiring layers** 2 are formed on a semiconductor substrate 1 and thereafter, an **SiOF** film 3 is formed on the whole surface of the substrate 1 by an HDP(High Density Plasma)-CVD method. The formation of this film 3 is performed under the condition where the amount of hydrogen, which is taken in the film 3, is suppressed. Specifically, the film 3 is formed using raw gas, which contains fluorine and oxygen and does not contain hydrogen. Or the film 3 is formed at a temperature higher than a temperature to reach the desorption peak of hydrogen in the heat-up and desorption characteristics of the film 3. After that, an SiO2 film 4 is formed using TEOS gas and a flattening of the surface of the film 4 is performed. Before an adhesive layer 6 is formed, a heat treatment is

performed and the hydrogen is made to release from the film 3. After a film having an action to occlude hydrogen in a Ti film or the like is deposited as the layer 6, a W film 7 is formed by a blanket WCVD method.

10/3,AB/30 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

06771813
MANUFACTURE FOR SEMICONDUCTOR DEVICE AND PLASMA CVD UNIT

PUB. NO.: 2000-357687 [JP 2000357687 A]
PUBLISHED: December 26, 2000 (20001226)
INVENTOR(s): MIYAJIMA HIDESHI
NAKADA RENPEI
KAWAI MOTONOBU
YAMADA NOBUHIDE
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 11-168619 [JP 99168619]
FILED: June 15, 1999 (19990615)

ABSTRACT

PROBLEM TO BE SOLVED: To form a lower permittivity **insulation film** without lowering reliability due to a degeneration layer by a method wherein temperatures of a semiconductor substrate are increased up to deposition temperatures of an **insulation film**.

SOLUTION: Not by a heating method by an oxygen ion impact, but by a heating method using a resistant heating heater, substrate temperatures are increased up to temperatures required for forming an **SiOF** film 4. Therefore, a CH3-SiO2 film is not oxidized. SiO4 and O2 as material gases are introduced into a reactive container at 20 SCCM and 40 SCCM, respectively, and the pressure is held at 5.0 mTorr, and induction power is set to be 2000 W, and the **SiOF** film 4 is formed on the entire surface by a high dense plasma CVD method. An Al **wiring** of a second layer and on is formed on the **SiOF** film 4. A degeneration layer which is a cause of generating HF is not formed, and therefore it is possible to form a lower permittivity interlayer **insulation film** by use of the high dense plasma CVD method without lowering reliability.

10/3,AB/31 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

06700431
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 2000-286262 [JP 2000286262 A]
PUBLISHED: October 13, 2000 (20001013)
INVENTOR(s): MATSUURA MASAZUMI
GOTO KINYA
APPLICANT(s): MITSUBISHI ELECTRIC CORP
APPL. NO.: 11-087521 [JP 9987521]
FILED: March 30, 1999 (19990330)

ABSTRACT

PROBLEM TO BE SOLVED: To provide the manufacture of a semiconductor device, which materializes one of such structures in which an F diffusion preventing film is not etched at formation of the metallic **wiring** of

an upper layer and that an **SiOF** film is not polished directly by CMP method, in a semiconductor device equipped with an F diffusion preventing film for preventing the F atoms in the **SiOF** film from diffusing into the metallic **wiring** of an upper layer.

SOLUTION: In this manufacture, a first layer metallic **wiring** 2, an **SiOF** film 3, and an F diffusion preventing film 6 are formed on the surface of the base layer 1 including a substrate, an element made on the substrate, and an **insulating layer** formed to cover the substrate and the element. For this F diffusion preventing film 6, it is sufficient to adopt a silicon nitride **film** or a silicon **oxide film** which includes Si-H bonding. Then, a spacer film 4 is made on the surface of the F diffusion preventing film 6, and the surface is flattened. Then, the second layer metallic **wiring** 5 is formed on the surface of the spacer film 4.

10/3,AB/32 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

06597371
WIRING STRUCTURE FOR SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME

PUB. NO.: 2000-183168 [JP 2000183168 A]
PUBLISHED: June 30, 2000 (20000630)
INVENTOR(s): YASUDA MAKOTO
APPLICANT(s): NEC CORP
APPL. NO.: 10-362468 [JP 98362468]
FILED: December 21, 1998 (19981221)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a multi-step **wiring** structure, capable of suppressing the generation and progress of EM phenomenon of Al.

SOLUTION: This **wiring** structure 40 is constituted by a lower **wiring** 44 formed on a base **insulating film** 42, an interlayer **insulating film** 46 formed on the **wiring** 44, a contact 48 which penetrates the layer 46, an upper **wiring** 50 connected with the **wiring** 44 via the contact 48. The layer 44 is constituted by an Al-Cu alloy layer which constitutes a **wiring** main body, a Ti layer 44b, and a TiN layer 44c. The layer 46 is constituted of a BPSG film 46a and an **SiOF** film 46b. The layer 50 is arranged between a contact and is constituted by a laminated barrier metal layer 52 having high (111) orientability, an Al-Cu alloy layer 50a constituting the **wiring** main body, a Ti layer 50b and a TiN layer 50c. The barrier metal layer 52 having high (111) orientability is constituted of a Ti layer 52a, having a film thickness of 20 nm and the TiN layer 52b the thickness of 40 nm for improving the (111) orientability and to suppress the generation and progress of EM phenomenon of Al.

10/3,AB/33 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

06426976
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 2000-012539 [JP 2000012539 A]

PUBLISHED: January 14, 2000 (20000114)
INVENTOR(s): KOYANAGI KENICHI
APPLICANT(s): NEC CORP
APPL. NO.: 10-169778 [JP 98169778]
FILED: June 17, 1998 (19980617)

ABSTRACT

PROBLEM TO BE SOLVED: To enable avoidance of deterioration of an adhesion between an interlayer **insulating film** and a barrier metal or **wiring** layer, when a **wiring** groove is made in a silicon **oxide film** containing fluorine as the interlayer **insulating film** and the **wiring** layer is formed in the groove through a barrier metal of Ti, etc.

SOLUTION: The manufacturing method includes steps of forming an **SiOF** film 102 on a substrate 101, forming an opening for **wiring** formation in the **SiOF** film, removing fluorine contained in the **SiOF** film from a surface of the opening, subjecting the fluorine-removed surface of the opening to an oxygen plasma process, and providing **wiring** metals 104 and 105 to the opening.

10/3,AB/34 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

06412806
ELECTRONIC DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-354464 [JP 11354464 A]
PUBLISHED: December 24, 1999 (19991224)
INVENTOR(s): MUROYAMA MASAKAZU
APPLICANT(s): SONY CORP
APPL. NO.: 10-157899 [JP 98157899]
FILED: June 05, 1998 (19980605)

ABSTRACT

PROBLEM TO BE SOLVED: To improve contact between a barrier metal layer and a metal layer which are formed in contact with **SiOF**, by laminating in sequence the barrier metal layer containing a specified metal and a metal **layer** on a silicon **oxide layer** containing fluorine.

SOLUTION: An interlayer **insulating film** 2 and a **wiring** layer 3 are formed on a semiconductor substrate 1, and hence the **wiring** layer 3 forms a step. Then, a silicon **oxide layer** 4 containing fluorine is formed thereon and the surface of the layer 4 is planarized. In the silicon **oxide layer** 4 containing fluorine, a connection hole 6 is made to the **wiring** layer 3 and is filled with a contact plug made of a barrier metal layer 7 and a metal layer 8. The barrier metal 7 contains at least one element selected from the group consisting of Ta, Zr, TaN, and ZrN. This strengthens a metal-oxygen atomic bond and a metal-fluorine atomic bond at the interface between the silicon **oxide layer** 4 containing fluorine and the barrier metal layer

10/3,AB/35 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

06193950
PREPARATION OF **WIRING** FOR SEMICONDUCTOR DEVICE

PUB. NO.: 11-135503 [JP 11135503 A]
PUBLISHED: May 21, 1999 (19990521)
INVENTOR(s): YAMADA YOSHIAKI
APPLICANT(s): NEC CORP
APPL. NO.: 09-294634 [JP 97294634]
FILED: October 27, 1997 (19971027)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method of preparing **wiring** for semiconductor devices, which suppresses reliability degradation caused by the diffusion of F out of an **SiOF** film and enhance resistance against electromigration, by heat-treating a metal layer which is composed mainly of aluminum to grow its crystal grains before forming the **SiOF** film.

SOLUTION: After a fist Al **wiring** 3 is formed, and thereon a Si **oxide film** 8 is formed by a PE-CVD method, heat treatment is performed at 400°C for 30 minutes. Average diameter of the grains of the Al alloy film increases by 2.2 times, from 0.5 μm before the heat treatment to 1.1 μm after the heat treatment. Besides, comparison of X-ray diffraction spectrum before and after the heat treatment shows that the intensity at the peak position for (111) plane of Al after the heat treatment is approximately 1.3 times that of before the heat treatment, indicating that the crystallographic plane of the crystal grains of the Al alloy film after the heat treatment is much more oriented to (111) plane as compared to before the heat treatment. The growth and the high orientation are not suppressed by the F of the **SiOF** film. By this method, it is possible to prevent degradation of electromigration resistance, enhancing reliability of the **wiring**.

10/3,AB/36 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

06170298
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-111845 [JP 11111845 A]
PUBLISHED: April 23, 1999 (19990423)
INVENTOR(s): MATSUNOU TADASHI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 09-271134 [JP 97271134]
FILED: October 03, 1997 (19971003)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor device which can suppress impurity diffusion and infiltration of water or hydroxyl ions for improving its reliability.

SOLUTION: Formed on an element isolation **insulating film** 11 is a **wiring** layer 20 of a plurality of first metal **wiring lines**. Formed on the **insulating film** 11 and the first

metallic **wiring** layer 20 are a silicon **oxide film** 31 added in high **concentration** of **fluorine**, a silicon nitride film 32 and an SiO2 film 33. The SiO2 film 33 higher in relative permittivity than the **SiOF** film 31 but lower than that of the silicon nitride film 32. Formed, in the **SiOF** film 31, silicon nitride film 32 and SiO2 film 33 is a via hole for connection with the first **wiring** layer 20. A W plug material 41 is embedded in the via hole. A second metal **wiring** layer 50 is formed on the SiO2 film 33.

10/3,AB/37 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

06099150
MULTILAYERED **WIRING** STRUCTURE AND ITS MANUFACTURE

PUB. NO.: 11-040669 [JP 11040669 A]
PUBLISHED: February 12, 1999 (19990212)
INVENTOR(s): YAMADA YOSHIAKI
APPLICANT(s): NEC CORP
APPL. NO.: 09-194429 [JP 97194429]
FILED: July 18, 1997 (19970718)

ABSTRACT

PROBLEM TO BE SOLVED: To embed an **insulating film** without any clearance between micro- **wiring** by using a PE-CVD (plasma chemical vapor phase epitaxy) method.

SOLUTION: After a first **wiring** 3 has been formed, a first interlayered **insulating film** 4 is formed to be thin, that is, almost 200 nm by an HDP(high density plasma)-CVD method. At that time, high-frequency bias is impressed to a silicon substrate 1, and sputter etching is simultaneously operated with film formation so that a successive taper shape whose upper part is wide and whose bottom part is narrow can be formed between a **wiring** 3. Afterwards, a second interlayered **insulating film** 5 is formed by a PE-CVD method, and at that time, gas including F as components for chemically etching the **insulating film**, for example, C2F6 is added so that an **SiOF** film or the like can be formed. The etching is carried out at the same time with the film formation, so that difference in level coatability can be made satisfactorily, and the base is formed into the successively taper shapes, so that the film formation can be attained without clearances between the micro-**wiring**.

10/3,AB/38 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

06084938
FORMATION OF **INSULATING FILM** AND SEMICONDUCTOR DEVICE

PUB. NO.: 11-026452 [JP 11026452 A]
PUBLISHED: January 29, 1999 (19990129)
INVENTOR(s): KOBAYASHI KINYA
FUKUDA TAKUYA
KATOU KIYOTAKA
APPLICANT(s): HITACHI LTD
APPL. NO.: 09-183475 [JP 97183475]
FILED: July 09, 1997 (19970709)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce the forming cost of an **insulating film** as much as possible, by combining a film forming a process using expensive SiH2F2 gas with another film forming process using inexpensive SiF4(+SiH4) gas.

SOLUTION: In a process 1, a plasma and, in its turn, various kinds of radicals are generated by ionizing SiH2F2 gas, O2 gas, and Ar gas by using a magnetic field generated from an electromagnet and microwaves, and parts of the insides of **wiring** grooves formed on the surface of a semiconductor wafer are filled up with an **SiOF** film. In a process 2, a plasma and, in its turn, various kinds of radicals are generated by introducing SiF4 gas and SiH4 gas to a film forming vessel, and parts of the insides of the **wiring** grooves formed on the surface of the semiconductor wafer are filled up with another **SiOF** film 23. When a film which is formed by a film forming method in which the processes 1 and 2 are combined together and has a small dielectric constant is used as an interlayer **insulating film**, the **wiring** delay or manufacturing cost of a semiconductor element resulting from an increased degree of integration can be suppressed as much as possible. Therefore, the manufacturing cost of highly integrated MPUs and DRAMs of the next generation can be reduced.

10/3,AB/39 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO

06020198
MULTILAYERED INTERCONNECTION STRUCTURE AND ITS FORMING METHOD

PUB. NO.: 10-303298 [JP 10303298 A]
PUBLISHED: November 13, 1998 (19981113)
INVENTOR(s): YOKOYAMA KOJI
YAMADA YOSHIAKI
KISHIMOTO KOJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-109291 [JP 97109291]
FILED: April 25, 1997 (19970425)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a multilayered interconnection structure which has an **SiOF film** as an interlayer **insulating film**, the excellent flatness and the high reliability by a method wherein an **oxide film** which does not contain fluorine and whose surface is levelled is formed on an **oxide film** which contains fluorine and fills the spaces between a plurality of **wiring** layers formed on a semiconductor substrate.

SOLUTION: 1st **wiring** layers 4 are formed on a semiconductor substrate with an **insulating film** therebetween. An **SiOF** film 6 containing fluorine and an intermediate **insulating film** 7 which does not contain fluorine are formed, and an SOG film 8 is formed and its surface is levelled. The surfaces of the SOG film 8 and the intermediate **insulating film** 7 are etched back by fluorine system gas, through-holes are formed at predetermined positions, and 2nd **wiring** layers electrically connected to the 1st **wiring** layers are formed. The intermediate **insulating layer** 7 improves the precision of

the etching back using a levelled film such as the SOG film 8. Further, the penetration of moisture into the **SiOF** film 6 which has a high moisture absorption property is avoided. The increase of the dielectric constant of the **SiOF** film 6 can be avoided and the corrosion of a through-hole part **wiring** caused by moisture can be eliminated.

10/3,AB/40 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO

05992759
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREFOR

PUB. NO.: 10-275859 [JP 10275859 A]
PUBLISHED: October 13, 1998 (19981013)
INVENTOR(s): YOKOYAMA KOJI
YAMADA YOSHIAKI
KISHIMOTO KOJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-080672 [JP 9780672]
FILED: March 31, 1997 (19970331)

ABSTRACT

PROBLEM TO BE SOLVED: To ensure contact of a plasma **SiOF oxide film** on a **wiring** and to improve embedding properties in a **wiring** space.

SOLUTION: An Al base metal 103 for **wiring** is spattered on a Si **oxide film** 102 to form a first **wiring** . A TiN antireflective **film** 105, a Si **oxide film** 106 are formed. A resist pattern 107 is formed in a known lithographic process and the Si **oxide film** 106 is patterned,. The Al base metal is etched using the patterned Si **oxide film** 106 as a mask. A plasma **SiOF** film is formed. On this process, the contact of the plasma **SiOF oxide film** on the **wiring** is improved, and its embedding properties on the **wiring** space are also improved.

10/3,AB/41 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

05861692
FORMING METHOD OF **INSULATING FILM**

PUB. NO.: 10-144792 [JP 10144792 A]
PUBLISHED: May 29, 1998 (19980529)
INVENTOR(s): SATO JUNICHI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-172696 [JP 97172696]
FILED: June 30, 1997 (19970630)

ABSTRACT

PROBLEM TO BE SOLVED: To form an **SiOF** film which is low in relative permittivity .epsilon. and capable of restraining Cu atom from being diffused into it even if a Cu **wiring** pattern is directly covered with it.

SOLUTION: A plasma CVD process is carried out using a mixed gas of silicon tetraisocyanate as Si-containing compound and fluorine-containing compound such as fluoride of element of oxygen rare gas fluoride, thiocarbonyl fluoride, thiocarbonyl perfluoride, carbonyl fluoride, sulfur fluoride or the like, whereby a **SiOF** film 23 is formed covering a Cu **wiring** pattern 22. As H gas is substantially excluded from material gas, H is not taken into the **SiOF** film 23, so that Si-OH groups which accelerate the diffusion of Cu are restrained from being produced in the film 23. Si and F are separately controlled in feed rate for a reaction system, so that Si contained in the film 23 is properly controlled so as to be at an adequate content level even if an enough amount of F is taken into the film 23, and the **SiOF** film 23 is lessened enough in permittivity.

10/3,AB/42 (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO

05815002
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 10-098102 [JP 10098102 A]
PUBLISHED: April 14, 1998 (19980414)
INVENTOR(s): MUROYAMA MASAKAZU
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-252541 [JP 96252541]
FILED: September 25, 1996 (19960925)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent the effects of fluorine upon an upper layer by providing a second inflating film, which has a little or no content of fluorine, on a first **insulating film**, which comprises a **silicon** fluoride **oxide film** and is so provided as to bury a **wiring** on a substrate, to suppress a capacity between the wirings and desorption of the fluorine from the surface of the **insulating film**.

SOLUTION: A first **insulating film** 14a of **silicon fluoride oxide** is so formed on a substrate 11 as to bury a **wiring** 13. A second **insulating film** 14b which has a fluorine content less than the first **insulating film** 14a is formed thereon. A contact hole 15 reaching the **wiring** 13 is formed through the first and second **insulating films** 14a and 14b. A contact layer 16 of titanium nitride is formed on the second **insulating film** 14b so as to coat the inner wall of the contact hole 15, and a plug forming layer 17 is formed on the contact layer 16 so as to fill the contact hole 15. Then the contact layer 16 and the plug forming layer 17 above the second **insulating film** 14b are removed, thereby a plug 17a is formed in the contact hole 15.

10/3,AB/43 (Item 16 from file: 347)
DIALOG(R)File 347:JAPIO

05758285
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 10-041385 [JP 10041385 A]
PUBLISHED: February 13, 1998 (19980213)
INVENTOR(s): MATSUMOTO AKIRA
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-190657 [JP 96190657]
FILED: July 19, 1996 (19960719)

ABSTRACT

PROBLEM TO BE SOLVED: To facilitate manufacturing of a buried **wiring** and effectively reduce the parasitic capacitance of the **wiring**, by forming an **insulation film** having a higher etching rate and lower specific dielectric const. than those of an **insulation film** beneath a **wiring** pattern on a region between the **wiring** patterns.

SOLUTION: The device has a first **insulation film** 11 on element regions on a semiconductor substrate 10 or **wiring** layer and **wiring** pattern 17' on this film 11. It also has a second **insulation film** 12 having a higher etching rate and lower specific dielectric const. than those of the first film 11 at least at a region formed between the patterns 17'. A first silicon **oxide film** 11 is deposited e.g. on the semiconductor substrate 10 having element regions, and **SiOF** film 12 is deposited thereon and used as an etching stopper to form **wiring** grooves 13. After forming contact holes 14, a second silicon **oxide film** 15, TiN **film** 16 and Al 17 are deposited to form the **wiring** 17'.

10/3,AB/44 (Item 17 from file: 347)
DIALOG(R)File 347:JAPIO

05720987
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 10-004087 [JP 10004087 A]
PUBLISHED: January 06, 1998 (19980106)

01/03/2002

INVENTOR(s): MUROYAMA MASAKAZU
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-154658 [JP 96154658]
FILED: June 14, 1996 (19960614)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor device having an **insulation film** having a low dielectric const. and superior embedding characteristic.

SOLUTION: A SiO(sub 2) film 2 and Al **wiring** pattern 3 are formed on a Si substrate 1, and this pattern 3 is covered with an interlayer **insulation film** 4 containing particles of a low dielectric const. inorganic compound in a resin. This compound is preferably one of **SiOF** , SiOBN, SiBN and BN. Adding of such particles of the compound reduces the resin's thermal expansion coefficient and raises its glass transition temperature

10/3,AB/45 (Item 18 from file: 347)
DIALOG(R)File 347:JAPIO

05645570
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 09-260370 [JP 9260370 A]
PUBLISHED: October 03, 1997 (19971003)
INVENTOR(s): SATO JUNICHI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-069743 [JP 9669743]
FILED: March 26, 1996 (19960326)

ABSTRACT

PROBLEM TO BE SOLVED: To enable forming a silicon **oxide**-based **insulating film** containing fluorine wherein dielectric constant is sufficiently reduced and contamination and deterioration of hot carrier resistance which are to be caused by addition gas are eliminated, by using material gas whose main components are tetraisocyanate silane and thiocarbonyl fluoride.

SOLUTION: A silicon **oxide**-based **insulating film** 4 containing fluorine is formed on a substrate 11 to be treated by using a CVD method using material gas whose main components are tetraisocyanate silane and thiocarbonyl fluoride. One or more kinds out of CSF(sub 2) and CSF(sub 4) are suitable for the thiocarbonyl fluoride. For example, a **wiring** layer 3 composed of Al-base metal is formed on a **layer insulating film** 2 on a semiconductor substrate 1 of Si or the like, and turned into the substrate 11 to be treated. The **layer insulating film** 4 which is composed of **SiOF** and whose dielectric constant is 3.3 is formed on the substrate 11 by using a plasma CVD method wherein Si(NCO)(sub 4) of 50sccm and CSF(sub 2) of 30sccm are used as material gas.

10/3,AB/46 (Item 19 from file: 347)
DIALOG(R)File 347:JAPIO

05645567
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 09-260367 [JP 9260367 A]
PUBLISHED: October 03, 1997 (19971003)
INVENTOR(s): SATO JUNICHI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-062250 [JP 9662250]
FILED: March 19, 1996 (19960319)

ABSTRACT

PROBLEM TO BE SOLVED: To enable forming an **oxide** silicon-based **insulating film** containing fluorine wherein dielectric constant is sufficiently reduced and contamination due to additional gas is eliminated, by using a CVD method using material gas whose main components are silane-based gas, oxidizing gas and chalcogen fluoride compound.

SOLUTION: An **oxide** silicon-based **insulating film** 4 containing fluorine is formed on a substrate 11 to be treated, by using a CVD method using material gas whose main components are silane-based gas, oxidizing gas and chalcogen fluoride compound. One or more kinds out of OF(sub 2), S(sub 2)F(sub 2), SF(sub 2), SF(sub 4), S(sub 2)F(sub 10), SeF(sub 4) and TeF(sub 4) are suitable for the chalcogen fluoride compound. For example, a **wiring** layer 3 composed of Al-based metal is formed on a **layer insulating film** 2 on a semiconductor substrate 1 of Si or the like, and it is made the substrate 11 to be treated. On the substrate 11, the **layer insulating film** 4 composed of **SiOF** is formed by using a plasma CVD method wherein SiH(sub 4) of 50sccm, O(sub 2) of 50sccm and S(sub 2)F(sub 2) of 30sccm are used as material gas.

10/3,AB/47 (Item 20 from file: 347)
DIALOG(R)File 347:JAPIO

05617508
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 09-232308 [JP 9232308 A]
PUBLISHED: September 05, 1997 (19970905)
INVENTOR(s): SATO JUNICHI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-035226 [JP 9635226]
FILED: February 22, 1996 (19960222)

ABSTRACT

PROBLEM TO BE SOLVED: To form a silicon **oxide** based **insulating film** with a practical deposition rate which film is free from contamination and contains fluorine, by using a CVD method material gas whose main component is compound composed of silane based gas, oxidizing gas, rare gas atoms and fluorine atoms.

SOLUTION: A substrate 11 to be treated is constituted by forming a **wiring** layer 3 composed of Al based metal constituted of **line** and space of specified width, on an interlayer **insulating film** 2 on a semiconductor substrate 1 of Si or the like. The substrate 11 is

mounted on the stage of a CVD equipment. A silicon **oxide** based **insulating film(SIOF**) containing fluorine is formed on the substrate 11 to be treated, by a CVD method using material gas whose main component is compound composed of silane based gas, oxydizing gas, rare gas atoms and fluorine atoms. Thereby an interlayer **insulating film** 4 is formed with a practical deposition rate which film is excellent in step coverage and composed of **SiOF** free from contamination of carbon and sulfur.

10/3,AB/48 (Item 21 from file: 347)
DIALOG(R)File 347:JAPIO

05533633
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 09-148433 [JP 9148433 A]
PUBLISHED: June 06, 1997 (19970606)
INVENTOR(s): YAMADA YOSHIAKI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-309108 [JP 95309108]
FILED: November 28, 1995 (19951128)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent the side part of lower-layer **wiring** from being etched even when a via hole projects from the **wiring**.

SOLUTION: After first **wiring** 3 is formed of an aluminum alloy 3, a first interlayer **insulating film** 4 composed of a thin silicon **oxide film**, and a second interlayer **insulating film** 5 composed of a **silicon** fluoride/**oxide film**, a via hole pattern is formed of a photoresist film 6 and the **silicon** fluoride/**oxide film**, namely, the second interlayer **insulating film** 5 is etched under a fluorine- poor etching condition. Under this condition, the first interlayer **insulating film** 4 composed of the silicon **oxide film** is hardly etched and, when the projecting amount of a via hole is smaller than the thickness of the film 4, the side part of the first **wiring** 3 is not etched by over-etching. Then the second interlayer **insulating film** 4 composed of the silicon **oxide film** is etched under a fluorine- rich etching condition. Since the silicon **oxide film** 4 has a thin thickness, the film 4 does not require any large over-etching amount and the side part of the **wiring** 3 is hardly etched.

10/3,AB/49 (Item 22 from file: 347)
DIALOG(R)File 347:JAPIO

05501205
LAYER INSULATING FILM

PUB. NO.: 09-116005 [JP 9116005 A]
PUBLISHED: May 02, 1997 (19970502)
INVENTOR(s): TO YOICHI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-269715 [JP 95269715]

01/03/2002

FILED: October 18, 1995 (19951018)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent **wiring** delay and **wiring** corrosion by preventing deterioration caused by moisture absorption of **silicon fluoride oxide** to be used as a **layer insulating film**.

SOLUTION: A **layer insulating film** 13 to be formed on a substrate 11 whereon wirinngs 12 are formed in a state of covering the **wiring** 12 consists of a **silicon** fluoride **oxide film** (a) and an amorphous silicon **oxide film** (b) to be arranged in a state of covering the top. A **layer insulating film** 16 to be arranged in a state of covering an upper layer **wiring** 15 of this **layer insulating film** 13 is made of two-layer structure of the **silicon** fluoride **oxide film** (a) and the amorphous silicon **oxide film** (b) of the top. Thereby, moisture in the atmosphere is interrupted by the amorphous silicon **oxide film** (b) so as to prevent moisture absorption of the **silicon** fluoride **oxide film** (a).

10/3,AB/50 (Item 23 from file: 347)
DIALOG(R)File 347:JAPIO

05467999

WIRING BOARD AND MANUFACTURE THEREOF

PUB. NO.: 09-082799 [JP 9082799 A]
PUBLISHED: March 28, 1997 (19970328)
INVENTOR(s): FURUSAWA KENJI
KUSUKAWA KIKUO
HONMA YOSHIO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI CHEM CO LTD [000445] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-235000 [JP 95235000]
FILED: September 13, 1995 (19950913)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a **wiring** board having small electrostatic capacitance between adjacent wirings and a flat **insulating layer** surface **coating** the **wiring** at a low cost by a method wherein a second **insulating layer** consisting of an organic silicon compound is formed on the surface of a first **insulating layer** and the intervals between the adjacent wirings are filled with both the first and second **insulating layers**.

SOLUTION: In order to reduce electrostatic capacitance between adjacent lower layer **wiring** patterns 2, intervals between the adjacent lower layer **wiring** patterns 2 are filled by using a first **insulating layer** 4a consisting of a low dielectric coefficient **SiOF** and a second **insulating layer** 5 consisting of organic SOG of a low dielectric coefficient. In order to lower the cost, a film thickness of the first **insulating layer** 4a is made not exceeding 40%, preferably not exceeding 20% of the intervals between the adjacent lower layer **wiring** patterns 2. For instant, in the case of 5.mu.m of the **wiring** interval, the thickness of the first **insulating layer** 4a is made not exceeding 0.2.mu.m, preferably not exceeding 0.1.mu.m.

10/3,AB/51 (Item 24 from file: 347)
DIALOG(R)File 347:JAPIO

05342760
DIELECTRIC BODY, MANUFACTURE THEREOF, AND SEMICONDUCTOR DEVICE

PUB. NO.: 08-298260 [JP 8298260 A]
PUBLISHED: November 12, 1996 (19961112)
INVENTOR(s): FUKUDA TAKUYA
KANAI FUMIYUKI
KATOU KIYOTAKA
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-040929 [JP 9640929]
FILED: February 28, 1996 (19960228)

ABSTRACT

PURPOSE: To enable a dielectric **film** which **insulates** the wirings of a semiconductor device from each other to be lessened in permittivity so as to relax the semiconductor device in **wiring** delay of signals.

CONSTITUTION: A **silicon oxyfluoride** film with bonds of Si-F and Si-O is used for insulating the **wiring** of a semiconductor device, SiF(sub 2)X(sub 2) (X=H, Cl, OCH(sub 3), OC(sub 2)H(sub 5), OC(sub 3)H(sub 7)) is used as reaction gas to form a dielectric film. Therefore, a **silicon oxyfluoride** film with bonds of Si-F and Si-O is smaller in permittivity than a **silicon oxyfluoride** film which contains bonds of Si-Si and O-F, so that a semiconductor device of this constitution lessened in **wiring** delay and enhanced in reliability can be manufactured.

10/3,AB/52 (Item 25 from file: 347)
DIALOG(R)File 347:JAPIO

05267060
METHOD OF FORMING **INSULATING FILM**

PUB. NO.: 08-222560 [JP 8222560 A]
PUBLISHED: August 30, 1996 (19960830)
INVENTOR(s): TAKEISHI SHUNSAKU
KUDO HIROSHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-029137 [JP 9529137]
FILED: February 17, 1995 (19950217)

ABSTRACT

PURPOSE: To provide a PCVD-**SiOF** film without applying low frequency by using tetraethyl orthosilicate, oxygen, and C(sub 2)F(sub 6) as material gas, and also, putting the volume flow rate ratio of oxygen gas to the tetraethyl orthosilicate gas to a value in specified range.

CONSTITUTION: A C(sub 2)F(sub 6) bomb 10 is connected through a pipe 9 to a material gas supply pipe 2. Moreover, an O(sub 2) bomb 13 is connected

through a pipe 12. Furthermore, a TEOS(tetraethylorthosilicate) source connected through a pipe 15. And, the volume flow rate ratio of oxygen gas to the tetraethyl orthosilicate gas is made twenty to forty. Here, if the volume flow rate ratio is less than twenty, the change with time becomes large, and it becomes about four after several times even if the permitivity at film growth is low at 3.5 to 3.7 or thereabouts. Moreover, when the volume flow rate ratio gets over forty, the film growth speed becomes slow, and besides the coverage to the difference in level of **wiring** drops.

10/3,AB/53 (Item 26 from file: 347)
DIALOG(R)File 347:JAPIO

05212101
METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

PUB. NO.: 08-167601 [JP 8167601 A]
PUBLISHED: June 25, 1996 (19960625)
INVENTOR(s): MUROYAMA MASAKAZU
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-332603 [JP 94332603]
FILED: December 13, 1994 (19941213)

ABSTRACT

PURPOSE: To form an **insulation film** low in the dielectric constant and the moisture absorption characteristic and excellent in the step coverage by a low output device by a method wherein the **insulation film** is formed of an organic Si compound having Si-F bond as material.

CONSTITUTION: An **insulation film** 23 is formed of an organic Si compound having Si-F coupling as material. As such organic Si compound, there are fluoroalkoxysilane, chain-like polysilane, annular polysilane and fluorosilane of a high order. The **insulation film** 23 is formed by a plasma CVD method with the use of such organic compound as material gas. For example, an interlayer **insulation film** 21 of an SiO(sub 2) film, etc., is formed on a semiconductor substrate 12 of an Si substrate, etc., and an Al **wire** 22 is pattered on this interlayer **insulation film** 21. Thereafter, an **SiOF** film 23 is formed under a specific condition by using a CVD device with the use of an organic Si compound having Si-F bond of, for example, difluorodiethoxysilane as material gas.

10/3,AB/54 (Item 27 from file: 347)
DIALOG(R)File 347:JAPIO

05193062
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 08-148562 [JP 8148562 A]
PUBLISHED: June 07, 1996 (19960607)
INVENTOR(s): USAMI TAKASHI
YOSHIMARU MASAKI
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or

Corporation), JP (Japan)
APPL. NO.: 06-285211 [JP 94285211]
FILED: November 18, 1994 (19941118)

ABSTRACT

PURPOSE: To realize both high performance and high reliability while using a fluorine added silicon **oxide film** as a **layer insulation film** by providing a film of low water absorption property which prevents hydrogen fluoride and fluorine from diffusing to at least either of an upper layer or a lower layer of the fluorine added silicon **oxide film**.

CONSTITUTION: A fluorine containing silicon **oxide film** (**SiOF film**) 17 is used as a **layer insulation film** of a semiconductor integrated circuit. In such a semiconductor device, a film 16 of low water absorption property which prevents hydrogen fluoride and fluorine from diffusing is provided to at least either of an upper layer or a lower **layer** of a first **insulation film** cosisting of the **SiOF** film 17 as a second **insulation film**. For example, a gate electrode 13, a **layer insulation film** 14 and a first metallic **wiring** layer 15 are provided on a semiconductor substrate 11 wherein an impurity diffusion layer 12 is formed. The **SiOF** film 17 is provide thereon with a silicon nitride film 16 of low water absorption property which prevents hydrogen fluoride and fluorine from diffusing through.

10/3,AB/55 (Item 28 from file: 347)
DIALOG(R)File 347:JAPIO

03588557
RECORDER AND RECORDING HEAD

PUB. NO.: 03-251457 [JP 3251457 A]
PUBLISHED: November 08, 1991 (19911108)
INVENTOR(s): TAMURA HIDEO
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-049873 [JP 9049873]
FILED: February 28, 1990 (19900228)
JOURNAL: Section: M, Section No. 1208, Vol. 16, No. 47, Pg. 144, February 06, 1992 (19920206)

ABSTRACT

PURPOSE: To record a high resolution securely for improving durability and reliability by using a kind of inorganic material as a **layer insulation** in a multilayer interconnection so as to contact a part of a second layer interconnection tightly with the inorganic material in a through-hole structure.

CONSTITUTION: Top of a silicon single crystal board 111 is filmed with an HfB(sub 2) layer 101 and an Al layer 102 as a heat generating resistance layer by means of sputtering and vapor deposition, so as to form a first conductive layer by patterning with etching. Next, a film of an **SiOf** (sub 2) layer is made as an oxidation-resistance protective layer of an electrothermal converter, and further, a film of a Ta layer 104 is made by means of sputtering as a cavitation- resistance protective layer and patterned. Then, it is coated with a photosensitive polyimide 105 as an

ink-resistance protective layer and patterned, and a film of an Al layer 107 is made thereon as a second conductive layer by means of the vapor deposition, and thereafter, patterning is performed. Further, after the board is coated with a protective layer 109 consisting of the photosensitive polyimide, patterning is performed. Thereafter, a roof 114 for forming a common liquid chamber 112 and a liquid **line** 113 is stuck by an adhesive and the like so as to make a recording head.

FILE 'REGISTRY' ENTERED AT 13:31:33 ON 03 JAN 2002
L1 41 SEA S (SI AND O AND F)/ELS AND 3/ELC.SUB

FILE 'HCAPLUS' ENTERED AT 13:32:01 ON 03 JAN 2002
L2 437 S L1
L3 433 S ((DIFLUOROSILANONE) OR (SILICON (W) OXYFLUORIDE) OR (SILICON (W) FLUORIDE (W) OXIDE) OR (HEXAFLUORODISILOXANE) OR (OCTAFLUOROTRISILOXANE))
L4 13424 S (FLUORINE OR F)(2A)(CONCENTRAT? OR PERCENT? OR PPM OR CENT OR WT OR WEIGHT)
L5 837643 S WIRE OR WIRES OR WIRING OR LINE OR LINES OR LINING
L6 1013 S (WIRE OR WIRES OR WIRING OR LINE OR LINES OR LINING)(3A)(GAP)
L7 230547 S (INSULAT? OR OXIDE OR DIELETRIC) (3A) (FILM# OR LAYER? OR COAT####)
L8 486 S L2 OR L3
L9 2 S L8(L)L4
L10 0 S L8(L)L6
L11 13 S L8(L)L5
D BIB AB 1-4
L12 3 S L8 AND L6
L13 57 S L8 AND L5

L14 4 S L13 AND L4
L15 39 S L13 AND L7
D BIB AB
D BIB AB 2-5

L16 177 S L8(L)L7

L17 0 S L16 AND L6
L18 20 S L16 AND L5
D BIB AB 1-2
L19 45 S L9 OR L11 OR L12 OR L14 OR L15 OR L18
L20 45 DUP REMOVE L19 (0 DUPLICATES REMOVED)
L21 45 S L20

L22 4 S L18 AND L4

L23 45 S L21 OR L22

=> D BIB AB 1-45

L23 ANSWER 1 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:840832 HCAPLUS
DN 135:351582
TI Semiconductor integrated circuit and its fabrication
IN Saito, Tatsuyuki; Ohashi, Naoshi; Imai, Toshinori; Noguchi, Junji; Tamaru, Takeshi
PA Hitachi Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 42 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001319928	A2	20011116	JP 2000-135041	20000508
	US 2001045651	A1	20011129	US 2001-850162	20010508
PRAI	JP 2000-135041	A	20000508		

AB A method for fabricating a semiconductor integrated circuit having a **wiring** resistant to migration involves prepg. a semiconductor substrate having a Si **oxide film** and a Si nitride film, forming a **wiring** recess in the **oxide** and nitride **films**, depositing a Cu **film** on the **oxide film** via a barrier layer, selectively removing the barrier layer and Cu film to form a **wiring**, and selectively forming a W cap film on the **wiring**. An integrated circuit fabricated by the above method is also described.

L23 ANSWER 2 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:781446 HCAPLUS
DN 135:337846
TI Design and fabrication of a semiconductor device comprising via holes and grooves formed by etching an organic low dielectric constant film
IN Nambu, Hidetaka
PA Japan
SO U.S. Pat. Appl. Publ., 16 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001034137	A1	20011025	US 2001-836286	20010418
	JP 2001308175	A2	20011102	JP 2000-120337	20000421
PRAI	JP 2000-120337	A	20000421		

AB A method is presented for manufg. a semiconductor device having a multi-layer **wiring** structure including a photo-resist pattern having a prescribed opening dimension which is formed on an interlayer **insulating film** composed of an org. low dielec. const. film and a Si-contg. **insulating film** durable to an NH3-based gas in which the Si-contg. **insulating film** is dry etched using the photo-resist pattern as a mask and then the org. low dielec. const. film is etched by dry etching with NH3 or an NH3-contg. gas using the Si-contg. **insulating film** as an etching mask to form an opening part having a high aspect ratio and a substantially vertical cross-section shape. The described method prevents bowing of the cross-section shape of a via hole formed in an org. low dielec. const. film as well preventing a shoulder drop effect in a Si-contg. **insulating film** used as an etching mask for the org. low dielec. const. film and provides a method for fabricating the semiconductor device which is capable of etching the org. low dielec. const. film with a high amt. of precision.

L23 ANSWER 3 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:710227 HCAPLUS
DN 135:265579
TI Fabrication of semiconductor device
IN Hiramatsu, Katsunori
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 16 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001267294	A2	20010928	JP 2000-72116	20000315

AB The title method involves forming a contact hole reaching a doped **layer** in a Si **oxide film** and plasma processing using a gas contg. hydrogen (such as steam) to convert a fluorocarbon polymer side-wall protective film to a hydrocarbon polymer side-wall protective film. The method is useful for suppressing the formation of under cuts of an underlayer **wiring** layer at the bottom of a contact hole in ashing with an O plasma during the formation of a contact hole in a Si **oxide film** by plasma etching using a pattern of a photoresist film and a fluorocarbon gas.

L23 ANSWER 4 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:489829 HCAPLUS
DN 135:69648
TI Semiconductor device having improved metal **line** structure and manufacturing method therefor
IN Kwon, Dong-Chul; Wee, Young-Jin; Shin, Hong-Jae; Kim, Sung-jJn
PA S. Korea
SO U.S. Pat. Appl. Publ., 13 pp., Division of U.S. Ser. No. 339,375.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001006255	A1	20010705	US 2001-785442	20010220
	KR 2000002928	A	20000115	KR 1998-23920	19980624
	US 6333260	B1	20011225	US 1999-339375	19990624
PRAI	KR 1998-23920	A	19980624		
	US 1999-339375	A3	19990624		

AB A semiconductor device having improved metal **line** structure has a 1st dielec. layer formed on a semiconductor substrate, a metal film pattern formed on the 1st dielec. layer, an interface protection layer on the metal film pattern, and a 2nd dielec. layer on the interface protection layer, in which the 2nd dielec. layer contains a reactive material, e.g., F, which is prevented by the interface protection layer from diffusing to the metal film pattern and reacting with the metal in the metal film pattern to form a damage film, e.g., metal fluoride, which is a highly resistive material that, if formed on the semiconductor device, would reduce the reliability of the metal film pattern and thus reduce the reliability of the semiconductor device as a whole.

L23 ANSWER 5 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:111469 HCAPLUS
DN 134:156450
TI CVD plasma process to fill contact hole in damascene process
IN Singh, Bhanwar; Templeton, Michael K.; Rangarajan, Bharath; Lyons, Christopher F.; Yedur, Sanjay K.; Subramanian, Ramkumar
PA Advanced Micro Devices, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6187666	B1	20010213	US 1999-328148	19990608

AB The present invention relates to a method for fabricating interconnecting **lines** and vias in a **layer** of **insulating** material. A via is formed in the **layer** of **insulating** material. A protective material is formed so as to be conformal to at least edges and sidewalls of the via, the protective material facilitating shielding of at least the edges and sidewalls of the via from a trench etch step. The trench etch step was performed to form a trench opening in the insulating material. The via and trench are filled with a conductive metal.

L23 ANSWER 6 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:29163 HCAPLUS
DN 134:94320
TI Fabrication of semiconductor device with low dielectric constant layer.
IN Yamagishi, Nobuhisa
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001007203	A2	20010112	JP 1999-175355	19990622

AB The process includes forming an **insulator layer** for covering 1st **wiring** on a semiconductor (e.g., Si) substrate, forming contact holes on the **insulator layer** and reaching 1st **wiring**, forming a plug material **layer** on the **insulator layer**, processing the plug material layer to form plugs protruded from the **insulator layer** and contacting with contact holes resp., and forming an interlayer **insulator layer** at the circumference side of the plugs for embedding the latter; the interlayer **insulator layer** is an org. low-dielec.-const. layer.

L23 ANSWER 7 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:874177 HCAPLUS
DN 134:35965
TI Method for fabricating a hybrid low-dielectric-constant intermetal dielectric (IMD) layer with improved reliability for multilevel interconnections
IN Chang, Weng; Cheng, Yao-yi
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6159842	A	20001212	US 1999-229382	19990111

AB A method for fabricating a hybrid low dielec. const. intermetal dielec. layer with improved reliability for multilevel elec. interconnections on integrated circuits is achieved. After forming metal **lines** for interconnecting the semiconductor devices, a protective **insulating layer** composed of a low-k F-doped oxide (k = 3.5) is deposited. A porous low-k spin-on dielec. layer (k <3) is formed in the **gaps** between the metal **lines** to further minimize the intra-level capacitance. A more dense low-k dielec. layer, such as FSG, is deposited on the porous layer to provide improved structural mech. strength and over the metal **lines** to provide reduced intra-level capacitance. Via holes are etched in the FSG and are filled with metal plugs and the method can be repeated for addnl. metal levels to complete the multilevel interconnections on the integrated circuit.

L23 ANSWER 8 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:723632 HCAPLUS
DN 133:289918
TI Semiconductor device having fluorine diffusion prevention layer and its manufacture
IN Matsuura, Masasumi; Goto, Kinya
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000286262	A2	20001013	JP 1999-87521	19990330
	US 2001021557	A1	20010913	US 2001-785248	20010220
PRAI	JP 1999-87521	A	19990330		
	US 1999-359654	A3	19990726		

AB An **insulating film** between an upper **wire** and a lower **wire** in the device comprises a lower F-contg. SiO2 (SiOF) layer, an intermediate layer, and an upper layer. The static capacitance of the **insulating film** is smaller in comparison with the case where a F-free SiO2 layer is used. The intermediate layer contains Si-N bonds or Si-H bonds or N atoms (e.g., a SiON layer) and prevents the diffusion of the F atoms in the SiOF layer. If the F atoms diffuse and reach the upper **wire** comprising Ti/TiN buffer layers and an Al alloy layer, a TiF compd. is generated and the upper **wire** comes off from the **insulating film**. The intermediate layer also prevents moisture from going into the SiOF layer while the upper layer is planed by CMP (chem. mech. polishing) using water.

L23 ANSWER 9 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:666680 HCAPLUS
DN 133:259345
TI Projection lithography photomask substrate and method of making
IN Berkey, George D.; Moore, Lisa A.; Pierson, Michelle D.
PA Corning Incorporated, USA
SO PCT Int. Appl., 80 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 3

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001027025	A1	20011004	US 2001-876194	20010606

PRAI US 1999-123861 P 19990312
US 1999-397572 A 19990916
US 1999-119805 P 19990212
US 1999-397577 A1 19990916
US 1999-159037 P 19991012
WO 2000-US3536 W 20000211

AB The present invention is a method of making a lithog. photomask and photomask blank. The method of making the lithog. photomask and photomask blank includes providing a **silicon oxyfluoride** glass tube having an OH content less than 50 ppm. The method further includes cutting the **silicon oxyfluoride** glass tube, flattening the **silicon oxyfluoride** glass tube, and forming the flattened cut **silicon oxyfluoride** glass tube into a photomask blank having a planar surface. The present invention includes a glass lithog. mask preform. The glass lithog. mask preform is a longitudinal **silicon oxyfluoride** glass tube that has an OH content <<leq 10 **ppm**, an **F wt. % concn**. <<geq 0.5 wt. %.

RE.CNT 11

L23 ANSWER 10 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:589860 HCAPLUS
DN 133:158719
TI Method of high density plasma CVD gap-filling with silica films
IN Shufflebotham, Paul Kevin; Weise, Mark
PA Lam Research Corporation, USA
SO U.S., 13 pp., Cont. of U.S. Ser. 623,825, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6106678	A	20000822	US 1998-83133	19980522
PRAI	US 1996-623825	B1	19960329		

AB A gap filling process of depositing a film of SiO2 in gaps on a substrate by generating plasma in a process chamber by energizing gas contg. Si, O and a heavy noble gas such as Xe or Kr. The gaps can have widths <0.5 .mu.m and aspect ratios >1.5:1. A substrate is supported on a substrate support wherein a gas passage supplies a temp. control gas into a space between opposed surfaces of the substrate and the substrate support, and the film is grown in the gaps on the substrate by contacting the substrate with the plasma. The Si reactant can be SiH4 and the O reactant can be pure O gas supplied by O2/SiH4 ratio of .ltoreq.1.05. The plasma can be a high d. plasma produced in an ECR or TCP reactor and the substrate can be a Si wafer including Al conductor **lines**.

L23 ANSWER 11 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:415489 HCAPLUS
DN 133:25382
TI Method of manufacturing self-aligned T-shaped gate through dual damascene in integrated-circuit fabrication
IN Chen, Yen-ming; Liu, Wei-jen; Lin, Shih-chi; Liu, Kuo-chou
PA Taiwan Semiconductor Manufacturing Co., Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6077733	A	20000620	US 1999-389885	19990903

AB A new method is provided to manuf. a T-shaped gate. A **layer** of **insulation** is deposited over a semiconductor surface (typically the surface of a substrate), a dual damascene structure contg. a via opening and a conducting **line** trench is created in the **layer** of **insulation**. A **layer** of sacrificial **oxide** is grown and subsequently removed (preventing initial surface defects and providing protection during subsequent steps of etching). A **layer** of gate **oxide** is selectively grown on the bottom of the dual damascene opening. A layer of polysilicon is deposited over the **layer** of **insulation** thereby including the dual damascene opening, the poly-Si is planarized down to essentially the top of the dual damascene structure and the insulation is removed from above the surface of the substrate in the regions surrounding the dual damascene structure leaving the dual damascene structure in

L23 ANSWER 12 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:271914 HCAPLUS
DN 132:272918
TI Method of sealing a semiconductor substrate
IN Balakrishnan, Sridhar
PA Intel Corporation, USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6054376	A	20000425	US 1997-1261	19971231

AB A method of sealing a substrate, comprising the steps of depositing a 1st amt. of a 1st material, having a 1st dielec. const., on the substrate to cover a bond pad and a metal line on the substrate and fill a **gap** between the metal **line** and the bond pad. The 1st amt. of material forming an inclined surface extending from an edge of the bond pad over the bond pad, depositing a 2nd amt. of the 1st material next to the inclined surface to cause a foot of the inclined surface to move along the inclined surface,. Etching the 1st material to cause the foot of the inclined surface to drop onto the bond pad, thereby cleaning a region of the bond pad adjacent the foot of the inclined surface, forming a layer on the 1st material and sealing on the cleared region of the bond pad,. The layer being of a 2nd material which is resistant to moisture and which has a 2nd dielec. const. which is greater than the 1st dielec. const., and etching the 2nd layer and the 1st material to clear an area of the bond pad within the sealing region.

L23 ANSWER 13 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:238037 HCAPLUS
DN 132:259275
TI Method of fabricating a semiconductor device having fluorine bearing oxide between conductive **lines**
IN Gardner, Mark I.; Kadosh, Daniel
PA Advanced Microdevices, Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6048803	A	20000411	US 1997-914658	19970819

AB A semiconductor device having relatively low permittivity F bearing oxide between conductive **lines** and a method for fabricating such a device is provided. At least two adjacent conductive **lines** are formed over a substrate. An **oxide layer** is formed between the adjacent conductive **lines**. A mask is formed over the **oxide layer** and selectively removed to expose a portion of the **oxide layer** between the adjacent conductive **lines**. A F bearing species is implanted into the exposed portion of the **oxide layer** to reduce the permittivity of the **oxide layer** between the adjacent conductive **lines**. The permittivity or dielec. const. of the **oxide layer** between the adjacent conductive **lines** can, for example, be reduced from .apprx.3.9 to 4.2 to .apprx.3.0 to 3.5.

L23 ANSWER 14 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:227216 HCAPLUS
DN 132:259235
TI Semiconductor device fabrication
IN Sugai, Kazumi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000100936	A2	20000407	JP 1998-268395	19980922
	JP 3164152	B2	20010508		

AB The title method involves depositing an **insulator film** such as SiO2, SiON, SiOF, parylene, benzocyclobutene, or hydrogen silsesquioxane on a semiconductor substrate, forming a **wiring** groove or vias in the **insulator film**, depositing a TaN film using (CH3)HNNH2 and a Ta halide such as TaCl5, TaF5, or TaBr5, and depositing a Cu film on the TaN film. A diffusion barrier is formed at a relatively low temp.

L23 ANSWER 15 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:166321 HCAPLUS
DN 132:201861
TI Semiconductor device with electromigration resistance and their manufacture
IN Iguchi, Manabu
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000077413	A2	20000314	JP 1998-248451	19980902

AB The barrier metal layers in the title semiconductor devices, comprising buried metal (e.g. Cu) **wirings**, consist of multilayered metals. The barrier metal layer contacting the **wiring** show strong adhesion with the **wiring** and that contacting the interlayer **insulator layer** is a diffusion prevention layer. The devices are manufd. by formation of a 1st and a 2nd **insulator layers** on a substrate, formation of a groove in the 2nd **insulator layer** utilizing the 1st **insulator layer** as an etch stopper, formation of a Cu diffusion prevention layer as the 1st barrier metal layer, formation of a metal layer showing strong adhesion with Cu as the 2nd barrier metal layer, and deposition of Cu until filling the groove, followed by chem. mech. polishing of the Cu and the 1st and the 2nd barrier metal layers down to the surface of the 2nd **insulator layer**. Another **insulator layer** having low dielec. const. may also be formed in between the 2 **insulating layers**. Cu **wirings** with excellent electromigration resistance are formed.

L23 ANSWER 16 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:140187 HCAPLUS
DN 132:272275
TI Study on the stability of HDP-SiOF film and IMD application for 0.25 .mu.m LSI device
AU Shin, H. J.; Kim, S. J.; Kim, B. J.; Kang, H. K.; Lee, M. Y.
CS Process Development, Samsung Electronics Co., Yongin city, S. Korea
SO IEEE Int. Interconnect Technol. Conf., Proc. (1998), 211-213 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y. CODEN: 68RVA8
DT Conference
LA English
AB A multilevel interconnection technol. using high-d.-plasma (HDP) SiOF film is demonstrated for 0.25 .mu.m LSI devices. A stable HDP-SiOF film is realized in the inter-metal dielec. (IMD). When HDP-SiOF has Si-F2 bonds and silicon dangling bonds, the film stress changes during thermal stressing. This unstable HDP-SiOF causes deformation of the underlayer metal by the film stress change. The device performance with stable HDP-SiOF film is improved by 12% redn. in **wiring** capacitance. In addn., gate oxide leakage characteristics are also superior to that of the conventional undoped silicate glass (USG). The stable HDP-SiOF film has been successfully applied to IMD layer for 0.25 .mu.m LSI device.

L23 ANSWER 17 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:34440 HCAPLUS
DN 132:72331
TI Production method of semiconductor device.
IN Koyanagi, Kenichi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000012539	A2	20000114	JP 1998-169778	19980617
	JP 3104750	B2	20001030		

AB The title method involves forming a SiOF **insulator film** on a substrate, forming openings for a **wiring** in the SiOF film, removing the F in the SiOF film via the surface of the openings, treating the surface of the openings with an O plasma, and forming a metal for the **wiring** in the openings. Specifically, F removal may be carried out by treating with a H plasma. A strong bonding between the metal and **insulator film** is obtained.

L23 ANSWER 18 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:814114 HCAPLUS
DN 132:43819
TI Electronic device having barrier metal layer and its manufacture method
IN Muroyama, Masakazu
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 11354464	A2	19991224	JP 1998-157899	19980605

AB The device is equipped with a F-contg. SiO2 layer successively coated with a barrier metal layer contg. Ta, Zr, TaN, and/or ZrN and a metal layer. The manuf. method involves (1) forming the SiO2 layer on a substrate and (2) successively forming the barrier metal layer and the metal layer thereon. The device shows improved adhesion between the SiO2 layer and the barrier metal layer and peeling prevention of the metal layer. The device may be useful for an interlayer **insulating film** or an inner **wiring** in a semiconductor device, etc.

L23 ANSWER 19 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:325610 HCAPLUS
DN 130:345924
TI Formation of **wiring** of semiconductor device.
IN Yamada, Yoshiaki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 11135503	A2	19990521	JP 1997-294634	19971027

AB The title method involves forming a **Wiring** of an Al-based metal layer, heat treating to grow the grains of the metal layer, and forming a SiOF film. Optionally, a F-frequency **insulator film** such as silica may be formed prior to the heat treatment. Specifically, the SiOF film may be formed using a silane gas (or TEOS), F-type gas such as CF4, C2F6, NF3, or SiF4 (or TEFS), and O2. The F diffusion into the **wiring** layer is prevented.

L23 ANSWER 20 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:234107 HCAPLUS
DN 130:260517
TI Interconnect structure with a low permittivity dielectric layer in semiconductor device fabrication
IN May, Charles; Cheung, Robin
PA Advanced Micro Devices, Inc., USA
SO PCT Int. Appl., 27 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9917359	A1	19990408	WO 1998-US6139	19980327
	W: JP, KR				
	RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 6117763	A	20000912	US 1997-939066	19970929
	EP 1019959	A1	20000719	EP 1998-913232	19980327
	R: DE, FR, GB, NL				
PRAI	US 1997-939066	A	19970929		
	WO 1998-US6139	W	19980327		

AB A method of making a semiconductor device includes forming a low permittivity dielec. layer over one or more conductive **lines** of a semiconductor device. The dielec. layer is made using a Si-contg. material having a relatively low permittivity including, for example, Si oxyfluoride (SiOyFx) and H silsesquioxane (HSQ). An optional **oxide layer** may be formed over the dielec. layer. At least a portion of the dielec. layer and/or the optional **oxide layer** is subsequently removed to form a planar dielec. layer having a contaminated surface layer. The contaminated surface layer is removed by, for example, exposing the surface to an acid, such as HF.

L23 ANSWER 21 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:816388 HCAPLUS
DN 130:89276
TI Fabrication of semiconductor device containing interlayer **insulating film** having a low dielectric constant
IN Miyajima, Shuji; Ui, Akio
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 10340897	A2	19981222	JP 1997-149154	19970606

AB The title process comprises: (1) prepg. a semiconductor substrate with a Ti-contg. metal **wiring** formed on its main surface; (2) forming a 1st oxidn. film contg. F on the main surface by using a 1st gas having a weak etching ability with respect to Ti; (3) decreasing the amt. of impurities remaining in the 1st oxidn. film, e.g., by discharge in an O-contg. gas; and (4) forming a 2nd oxidn. film contg. F on the 1st oxidn. film by using a 2nd gas having an etching ability with respect to Ti stronger than that of the 1st gas. The 2nd oxidn. film is prepd. by high-d. plasma CVD. Etching damage of the **wiring** during the formation of the 2nd **insulating film** is prevented, and the dielec. const. of the **insulating film** can be decreased.

L23 ANSWER 22 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:735333 HCAPLUS
DN 130:31796
TI Multilayer interconnection structure and its formation method.
IN Yokoyama, Takashi; Yamada, Yoshiaki; Kishimoto, Koji
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10303298	A2	19981113	JP 1997-109291	19970425
	JP 3109449	B2	20001113		
	CN 1198015	A	19981104	CN 1998-101625	19980422
	US 2001003060	A1	20010607	US 1998-66115	19980423
	US 6287956	B2	20010911		
PRAI	JP 1997-109291	A	19970425		

AB A planar multilayer interconnection structure comprises a no. of **wiring** layers on a semiconductor substrate, an **oxide film** contg. F for filling between the **wiring layers**, and an **oxide** planar **film** free of F on the **oxide film** contg. F. Addnl., a SOG film may be formed on the **oxide** planar **film**. A method for forming the above structure involves forming a 1st **wiring** layer on a semiconductor substrate via an **insulator film**, forming a SiOF **film**, forming a middle **insulator film** of an **oxide film** free of F, forming a SOG film to planarize the middle **insulator film**, dry etching back the SOG and middle **insulator films** using a F-contg. gas such as CF4, C2F6, NF3, or SiF4, forming a contact hole to reach the 1st **wiring** layer, and forming a 2nd **wiring** layer contacting the 1st **wiring** layer.

L23 ANSWER 23 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:542741 HCAPLUS
DN 129:169188
TI Self-aligned contact **wiring** process for Si devices
IN Bronner, Gary B.; Gambino, Jeffrey P.
PA International Business Machines Corp., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5792703	A	19980811	US 1996-619047	19960320

AB A method of making elec. contacts to device regions in a substrate is taught. A first set of contacts are self-aligning and borderless and a second set of contacts are bordered. The method comprises the steps of providing a first **insulating layer** over the substrate and forming the first set of contacts in a self-aligned and borderless manner. This is followed by forming a second **insulating layer** over said first **insulating layer**, in which the second set of contacts that are bordered to the gate electrode and peripheral diffusions are formed through the first and second **insulating layers**. In addn., bordered contacts to the first set of borderless contacts are formed through the second **insulating layer**.

L23 ANSWER 24 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:479657 HCAPLUS
DN 129:103086
TI Inductively coupled plasma CVD of dielectric films
IN Shufflebotham, Paul Kevin; McMillin, Brian; Demos, Alex T.; Nguyen, Huong; Berney, Butch; Ben-Dor, Monique
PA Lam Research Corp., USA
SO PCT Int. Appl., 44 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9828465	A1	19980702	WO 1997-US22987	19971222
	W: JP, KR				
	RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 6184158	B1	20010206	US 1996-772374	19961223
	EP 953066	A1	19991103	EP 1997-953209	19971222
	R: AT, DE, FR, GB, IT, NL, IE				
	JP 2001507081	T2	20010529	JP 1998-528868	19971222
	TW 432493	B	20010501	TW 1997-86119628	19980212
	US 2001019903	A1	20010906	US 2001-775664	20010205
PRAI	US 1996-772374	A	19961223		
	WO 1997-US22987	W	19971222		

AB A dielec. film is deposited on a substrate in a process chamber of an inductively coupled plasma-enhanced CVD reactor. Gap filling between elec. conductive lines on a semiconductor substrate and depositing a cap layer are achieved. Films having significantly improved phys. characteristics including reduced film stress are produced by heating the substrate holder on which the substrate is positioned in the process chamber.

L23 ANSWER 25 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:351424 HCAPLUS
DN 129:75143
TI Prevention of fluorine-induced metal wire deterioration in semiconductor integrated circuits
IN Coney, Edward C., III; Lee, Hyun K.; Mcdevitt, Thomas L.; Stamper, Anthony K.
PA International Business Machines Corp., USA
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10144793	A2	19980529	JP 1997-293792	19971027
	US 6310300	B1	20011030	US 1996-744846	19961108
	US 5930655	A	19990727	US 1997-937622	19970925
	US 6066577	A	20000523	US 1997-937367	19970925
	CN 1182956	A	19980527	CN 1997-120067	19971007
	US 6214730	B1	20010410	US 1999-257372	19990225
PRAI	US 1996-744846	A	19961108		
	US 1997-937367	A3	19970925		
	US 1997-937622	A3	19970925		

AB The invention relates to a process for improving the resistance of metal conductors in semiconductor integrated circuits to the damages caused by F attack, wherein the metal layer is isolated from the F-contg. dielec. material by a F-free barrier layer.

L23 ANSWER 26 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:260389 HCAPLUS
DN 128:329364
TI A 0.7-.mu.m-pitch double level Al interconnection technology for 1-Gbit DRAMs using SiO2 mask Al etching and plasma enhanced chemical vapor deposition SiOF
AU Yokoyama, Takashi; Yamada, Yoshiaki; Kishimoto, Koji; Usami, Tatsuya; Kawamoto, Hideaki; Ueno, Kazuyoshi; Gomi, Hideki
CS ULSI Device Development Lab., NEC Corporation, Kanagawa, 229-11, Japan
SO Jpn. J. Appl. Phys., Part 1 (1998), 37(3B), 1140-1144
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB A 0.7-.mu.m-pitch double level aluminum (Al) interconnection technol. on a 1-.mu.m-high step is established for 1-Gbit dynamic random access memories (DRAMs). A SiO2 film which has a high resistance to Al etching was used as the mask layer. 0.35-.mu.M-width Al **wirings** were fabricated even on a 1-.mu.m-high step. 0.2-.mu.M-spaces (aspect ratio=2.5) between the taper shaped Al **lines** were filled, for the first time, by a plasma enhanced chem. vapor deposition (PECVD) fluorine doped silicon **oxide** (SiOF) **film** (.epsilon.=3.9). The SiOF film capped with the PECVD SiO2 film has enough stability for the process integration. It was confirmed that these technologies can be applied to a double level l interconnection using a 0.3-.mu.m-diam. tungsten (W) plug.

L23 ANSWER 27 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:227123 HCAPLUS
DN 128:303002
TI Semiconductor device having **wiring** buried in **insulator film** and its fabrication method
IN Muroyama, Masakazu
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 10098102	A2	19980414	JP 1996-252541	19960925

AB The title device comprises a 1st **insulator film** of a fluorinated silicon **oxide film** having a buried **wiring** and a 2nd **insulator film** of a fluorinated silicon **oxide film** having a F content less than that for the 1st **insulator film** or from a film free of F. A method for fabricating the device involves CVD of the 1st and 2nd **insulator films**. The **insulator films** has a high bonding strength.

L23 ANSWER 28 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:799916 HCAPLUS
DN 128:109153
TI Integration of a stack of two fluorine doped silicon **oxide** thin **films** with interconnect metalization for a sub-0.35 .mu.m inter-metal dielectric application
AU Baud, L.; Passemard, G.; Gobil, Y.; M'Saad, H.; Corte, A.; Pires, F.; Fugier, P.; Noel, P.; Rabinzohn, P.; Beinglass, I.
CS chemin de la Dhuy, Applied Materials, 38240 Meylan, 11B, Fr.
SO Microelectron. Eng. (1997), 37/38, 261-269
CODEN: MIENEF; ISSN: 0167-9317
PB Elsevier Science B.V.
DT Journal
LA English
AB F doped Si **oxide films** were deposited on HDP-CVD system and on PECVD system to realize a stack to be integrated in metal **lines**' architecture. Resistance to moisture absorption of both films was studied by film exposure in humid atm. for 1 wk followed by an annealing. Phys. properties of uncapped FSG films were measured before and after test in humid atm. and after outgassing. Moisture absorption is increasing with the F content for both films, and this moisture absorption creates F desorption, clearly visible after outgassing, for **concn**. >6 at.% **F**. The mech. stress, d. and refractive index also follow the stability evolution. A very stable process was confirmed for both FSG HDP and PECVD layers for a **F concn**. <6 at.%. Finally it was demonstrated the capability to reach a dielec. const. at 3.5 .+-. 0.05 for FSG HDP-CVD films. In a 2nd step, integration was evaluated. No problem occurs for chem. mech. polishing of FSG films, via etching, metal barrier adhesion and W plug metalization leading to a partial integrated structure. These results are very promising for the integration of FSG films as intermetal dielecs. for devices.

L23 ANSWER 29 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:772566 HCAPLUS
DN 128:56387
TI Formation method of **insulator film**.
IN Muroyama, Masakazu
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09312333	A2	19971202	JP 1996-126618	19960522

AB A method for forming an **insulator film** to bury a **wiring** on a substrate involves plasma CVD of a Si **oxide** underlay **film** optionally contg. a low **concn**. of **F** and then a Si fluoride **oxide** overlay **film**. Specifically, the underlay and overlay films may be formed using gases having Si-H and Si-F bonds, resp. A film having a low water permeability is formed.

L23 ANSWER 30 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:664577 HCAPLUS
DN 127:313855
TI Etching process for offset **insulating films** in

excellent pattern reliability
IN Tatsumi, Tetsuya
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09266196	A2	19971007	JP 1996-73465	19960328

AB In the process for semiconductor device fabrication, the angles between the etched surfaces and resist-mask sidewalls are controlled to be (i) larger than the retreating angles of **line** width of resist masks and (ii) smaller than the deposition angles of fluorocarbon polymers on the sidewalls.

L23 ANSWER 31 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:533581 HCAPLUS
DN 127:154446
TI Methods and apparatus for providing an absorbing, broad band, low brightness antireflection coating
IN Adair, Robert W.; Lefebvre, Paul M.; Kurman, Eric W.
PA Optical Coating Laboratory, Inc., USA
SO PCT Int. Appl., 30 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PRAI US 1996-595350	A	19960201		
WO 1997-US1341	W	19970128		

AB Antireflective coatings are described which comprise a first layer of a transition metal oxynitride and a transparent layer arranged on the absorbing layer. The antireflection coatings preferably have brightness values less than or equal to about 0.22, and most preferably less than or equal to about 0.15. Due to the simplicity of the design and the suitability and efficiency of the deposition of the materials in an in-**line** d.c. reactive magnetron sputtering process, the high performance, absorbing, elec. conductive, and contrast-enhancing antireflection coatings can be produced in a cost-effective manner.

L23 ANSWER 32 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:385276 HCAPLUS
DN 127:43473
TI Bilayered interlayer **insulating film** with high moisture resistance
IN Tsutsumi, Yoichi
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09116005	A2	19970502	JP 1995-269715	19951018

AB The **insulating film**, formed on a **wiring**, comprises a Si fluoroxide film and an amorphous Si **oxide**

film coating. The **insulating film** inhibits generation of fluoric acid which causes a corrosion of the **wiring**.

L23 ANSWER 33 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:324220 HCAPLUS
DN 127:27861
TI Multilayer **wiring** board and its manufacture
IN Furusawa, Kenji; Kusukawa, Kikuo; Honma, Yoshio
PA Hitachi, Ltd., Japan; Hitachi Chemical Co., Ltd.
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09082799	A2	19970328	JP 1995-235000	19950913

AB The **wiring** board has several metal (alloy) **wiring** patterns whose sides are successively laminated with a F-contg. Si compd. elec. **insulating layer** and an org. Si compd. elec. **insulating layer** to bury the spaces between the patterns. The manuf. of the above **wiring** board involving chem. mech. polishing with a Ce oxide particle-contg. polisher is also claimed. Flat **wiring** boards with low elec. capacitance between neighboring **wirings** are obtained by the method at low cost.

L23 ANSWER 34 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:124002 HCAPLUS
DN 126:138061
TI Manufacture of fluorine-containing silicon **oxide** electric **insulating film** by plasma vapor deposition
IN Tamura, Yoshihiro
PA Anelva Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08330293	A2	19961213	JP 1995-156974	19950530

AB The title method comprises (1) introducing gaseous O to a deposition chamber where a substrate is placed or to a plasma generating chamber which is spaciously continuous to the deposition chamber to form O plasma, (2) introducing a F-contg. Si compd. gas (X) and a H-contg. a Si compd. gas (Y) there to form a F-contg. Si **oxide** elec. **insulating** thin **film** on the substrate by plasma vapor deposition while the flow of X to (X + Y) is controlled to 1-50%. In the above method, the elec. **insulating film** may be formed only from X in the presence of previously formed O and H plasma from gaseous O and H while the flow of H to X is controlled to 200-400%. The app. for the above methods is also claimed. The method is useful for lamination of elec. **insulating films** on **wiring** patterns in elec. circuits without etching them.

L23 ANSWER 35 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:635078 HCAPLUS
DN 125:263192

TI Semiconductor devices and manufacture thereof with **silicon fluoride oxide films**
IN Yahiro, Kazuyuki
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08203892	A2	19960809	JP 1995-12410	19950130
JP 3192903	B2	20010730		

AB The title process comprises formation of a **insulating film** on a **wiring** layer over the semiconductor substrate and deposition of a reflow SiO2 film by reaction of SiH4, H2O2, and a radical F-system gas which is supplied through a microwave waveguide at .apprxeq.665 Pa and -10 to +10.degree. in formation of an interlayer **insulating film**. The reflow SiO2 film having sp. dielec. const. .apprxeq.3.6 is obtained.

L23 ANSWER 36 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:508791 HCAPLUS
DN 125:156208
TI Semiconductor apparatus with interlayer **insulating film** structure
IN Hasegawa, Toshiaki
PA Sony Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08162528	A2	19960621	JP 1995-3727	19950113
PRAI JP 1994-238821		19941003		

AB The app. comprises an **insulating** substrate successively **coated** with a **wiring** and 1st **insulating film**, and 2nd **insulating film** with lower sp. inductive capacity on the **wiring**. The app. may comprises 3rd **insulating film** (under the **wiring**) made of Si (nitr)oxide, and/or Si nitride, and 4th **insulating film** (under the 3rd **insulating film**) made of F-contg. Si oxide, polysiloxane, poly(p-xylylene), fluorocarbons, and/or polyimide. The **wiring** has high reliability due to inhibited corrosion of the 2nd **insulating film** and poisoned via.

L23 ANSWER 37 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:468973 HCAPLUS
DN 125:130139
TI Semiconductor device having fluorine-containing interlayer **insulating film** and its manufacture
IN Usami, Takashi; Yoshimaru, Masaki
PA Oki Electric Ind Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08148562	A2	19960607	JP 1994-285211	19941118

AB The title method involves successive lamination of (1) a **wiring** pattern, (2) an elec. insulating F-contg. Si **oxide film**, and (3) another elec. **insulating film**, which shows low water absorption and prevents diffusion of HF and F, without exposure to atm. on a semiconductor substrate. The device is also claimed. Diffusion of Hf and F, which causes corrosion of metal **wirings** in the device and increase of interlayer capacitance, is prevented by the method.

L23 ANSWER 38 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:362594 HCAPLUS
DN 125:101163
TI Instability of Si-F bonds in fluorinated silicon **oxide** (SiOF) **films** formed by various techniques
AU Homma, Tetsuya
CS ULSI Device Development Laboratories, NEC Corporation, 1120 Shimokuzawa, Sagamihara, Kanagawa, 229, Japan
SO Thin Solid Films (1996), 278(1-2), 28-31
CODEN: THSFAP; ISSN: 0040-6090
DT Journal
LA English
AB Instability of Si-F bonds in fluorinated silicon **oxide** (SiOF) **films** is studied. Al **wiring** corrosion and underlayer SiO2 etching problems are the major issues for the use of SiOF interlayer dielec. films. To clarify the mechanism, three kinds of SiOF films have been used for this study. They are: (i) a fluorinated silicon **oxide** (SiOF) **film** prepd. by room-temp. chem. vapor deposition (RTCVD) using fluorotriethoxysilane and pure water as gas sources; (ii) a fluorinated spin-on-glass (SOG) film prepd. by fluorotrialkoxysilane vapor treatment (FAST); and (iii) a room-temp. liq. phase deposition (LPD) SiOF film. The initial refractive indexes for the RTCVD-SiOF, FAST-SOG and LPD-SiOF films are 1.400, 1.398 and 1.433, resp. After conducting a pressure cooker test (PCT) at 125.degree. for 520 h, the refractive indexes for the RTCVD-SiOF, FAST-SOG and LPD-SiOF films increase to 1.450, 1.440 and 1.436, resp. The Si-O bond peak absorption coeff. for the LPD-SiOF film decreases at the early stage of PCT, but those for the RTCVD-SiOF and FAST-SOG films increase at the early stage of PCT. The initial Si-F bond peak absorption coeff. for the RTCVD-SiOF film is much higher than those for the LPD-SiOF and FAST-SOG films. It decreases drastically in the PCT time ranging from 0 to 140 h. The Si-F bond peak absorption coeffs. for the FAST-SOG and LPD-SiOF films show a slow redn., as compared with that for the RTCVD-SiOF film at the early stage of PCT. Although the OH peak absorption coeffs. for the RTCVD-SiOF

and FAST-SOG films increase at the early stage of PCT and level off at 50 h, that for the LPD-SiOF film increases at 306 h. After conducting 520 h PCT, **concns**. of **fluorine** atoms for the RTCVD-SiOF and FAST-SOG films decrease by three orders and two orders of magnitudes, resp. However, the LPD-SiOF film has a limited change in the **fluorine concn**., as compared with those for the RTCVD-SiOF and FAST-SOG films. The thicknesses for all of the films remain almost unchanged after PCT for 520 h.

L23 ANSWER 39 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:302397 HCAPLUS
DN 124:358415
TI Semiconductor integrated circuit
IN Ichikawa, Jinko; Tsuneno, Katsumi; Masuda, Hiroo; Sato, Hisako; Nakamura, Takahide; Kunitomo, Hisaaki
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08064677	A2	19960308	JP 1994-201226	19940826

AB The circuit consists of a semiconductor substrate having pitch wirings with width .gtoreq.0.8 .mu.m and thickness 0.3-1.0 .mu.m. The circuit showed high transistor d.

L23 ANSWER 40 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:262660 HCAPLUS
DN 124:304245
TI Reliable leads for semiconductor devices and their fabrication
PA Texas Instruments Inc., USA
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08046046	A2	19960216	JP 1995-134298	19950531
US 5510293	A	19960423	US 1994-251822	19940531
PRAI US 1994-251822		19940531		

AB Semiconductor devices are provided with reliable leads by forming at least a pair of metal lead **wires** on the device substrate, depositing a material with a low dielec. const. (< 3.5) at least between the lead **wires**, and depositing a thermally conductive **insulating layer** comprising AlN and/or Si3N4 at least over the leads; the thermally conductive layer acts to conduct heat away from the leads. By conducting heat away from the leads, the chances of the leads breaking is reduced and the reliability of the leads is improved.

L23 ANSWER 41 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:248491 HCAPLUS
DN 124:304417
TI Manufacture of semiconductor device
IN Murase, Hiroshi
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.

liq.-phase deposition (LPD) method at 15.degree.. The F is uniformly distributed in the bulk of the LPD oxide. The F incorporation as well as the qual. properties can be accurately controlled by varying the amt. of H2O added. A high temp. process has considerable effect on the low temp. fluorinated oxide. FTIR and XPS spectra show that Si-F and SiO-H bonds can restructure with densification at higher thermal annealing temp., and that restructuring is a function of temp. Film densification with increasing temp. is also discussed in terms of Si-O-Si bond angle and Si-Si bond length.

L23 ANSWER 44 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:150873 HCAPLUS
DN 120:150873
TI Flow characteristics of silicon **oxide** fluoride **films** in room temperature chemical vapor deposition utilizing fluoro-trialkoxy-silane group and pure water as gas sources
AU Homma, Tetsuya; Murao, Yukinobu; Yamaguchi, Ryuichi
CS ULSI Dev. Dev. Lab., NEC Corp., Sagamihara, 229, Japan
SO J. Electrochem. Soc. (1993), 140(12), 3599-603
CODEN: JESOAN; ISSN: 0013-4651
DT Journal
LA English
AB The flow characteristics of SiOxFy films formed by room temp. CVD for interlayer dielecs. of multilevel interconnections were studied. The room temp. CVD technique uses fluoro-trialkoxy-silane group (FTAS, FSi(OR)3, R: alkyl group) and pure H2O as gas sources. The films deposited using fluoro-tri-normalpropoxy-silane (TFNPS, FSi(n-OPr)3) have better flow surface profiles on Al **wirings** than others such as fluoro-trimethoxy-silane (FTMS), fluoro-triethoxy-silane (FTES), and fluoro-tri-isopropoxy-silane (FTIPS). From the speculated SiOxFy films deposition mechanism, probably the flow surface profiles are due to the fluorosilanol oligomer flow. The fluorosilanol oligomers flow may occur when the surface migration velocity of the oligomers with reaction byproducts is larger than the polymn. velocity at the trenches between Al **wirings**. The reasons why the SiOxFy films deposited using FTNPS have better flow surface profiles are considered as due to the fact that normalpropyl alc., reaction byproduct, has lower vapor pressure (20 torr) than other reaction byproducts such as Me alc. (125 torr), Et alc. (58 torr), and isoPr alc. (44 torr) at the deposition temp. (25.degree.), and that the polymn. velocity is smaller than those using FTMS, FTES, and FTIPS. Similar flow surface profiles are obtained by adding normalpropyl alc. to FTES during the film deposition. Although the deposition rate and etching rate for the SiOxFy films depend on the C no. in the alkyl group of FTAS, the nature and quality of the Si-O bonds do not depend on the C no.

L23 ANSWER 45 OF 45 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:202862 HCAPLUS
DN 118:202862
TI Room-temperature chemical vapor deposition silicon **oxide** fluoride (SiOF) **film** formation technology for the interlayer in submicron multilevel interconnections
AU Homma, Tetsuya; Yamaguchi, Ryuichi; Murao, Yukinobu
CS NEC Corp., ULSI Dev. Dev. Lab., Sagamihara, 229, Japan
SO J. Electrochem. Soc. (1993), 140(3), 687-92
CODEN: JESOAN; ISSN: 0013-4651
DT Journal
LA English
AB A new interlayer dielec. film formation technol. for multilevel

interconnection by catalytic chem. vapor deposition has been developed. This technique utilizes fluorotriethoxysilane [FSi(OC2H5)3] and water vapor as gas source. Films deposited at 25.degree. have remarkably good properties, such as lightly bonded Si-O networks with no OH radicals, large d. value (2.20 g/cm3), small residual stress (50 MPa), low leakage current, and small dielec. const. (3.7), although the film contains residual fluorine and carbon atoms with 5.3 .times. 1021 and 2 .times. 1021 atoms/cm3, resp. Based on the film characterization results, the reaction sequence for the film deposition is: hydrolysis of fluorotriethoxysilane monomers, formation of siloxane oligomers with reaction byproduct (alc.), adsorption of the oligomers to the wafer surface, and then polymn. Elec. conduction mechanism study revealed that Schottky emission is dominant for the elec. conduction through the film. Also the deposition film thickness is independent of Al **wiring** width and is completely isotropic with no crack or keyhole in the film.

US 0986373705P1

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